.....a total solution for
Educational Lab Trainers

DIGITAL & ANALOG TRAINER KIT

DTK-01A

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INTRODUCTION

This Digital/Analog Trainer has been designed with the idea of providing basic facilities essential for conducting simple experiments in the laboratory. Using these facilities one can get oneself familiarized with the various digital ICs. The system is suitable for conducting experiments on TTL as well as CMOS ICs.

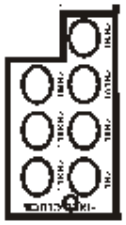
TECHNICAL SPECIFICATIONS

- 10/16 TTL/CMOS compatible Logic Level Inputs.
- 10/16 Dual color LEDs Logic level indicators for inputs.
- 10/16 LEDs Logic Level Indicators for outputs.
- 1Hz, 10Hz, 100Hz, 1KHz, 10KHz, 100KHz, 1MHz fixed Clock Generator.
- Sine, Square, Triangle Function Generation up to 30 KHz.
- Facility for Single Pulsar Generation by a push button switch.
- Logic probe to check logic low, logic high pulse.
- Facility for 4 digit seven segment display.
- On-board Voltage Panel Meter (Optional).
- On-board 1280 TIE points Bread Board.
- 20 Pin ZIF socket for IC experiment (Optional).
- In-Built Power Supply of +5V, ±12V.
- In-Built Variable DC Power Supply of ±1.25 to ±15V.
- In-Built AC Power Supply of 15V-0-15V.

HARDWARE DESCRIPTION

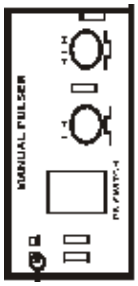
Clock Generation (Block-12)

The system uses a IC 74LS04 analog with a 4.00MHz crystal to generate a clock of 4MHz which is then divided by IC 74LS93 to achive 1MHz clock frequency. The Clock level is made compatible with TTL and CMOS levels. This clock is then divided using ICs CD4518 and CD4013B to generate the frequencies of 1Hz, 10Hz, 100Hz, 1 KHz, 10 KHz, 100 KHz & 1 MHz are brought out at six 2mm terminals through no inverting buffers.



Manual Clock (Block-9)

The system uses a CMOS NAND GATE IC CD4011 to generate a manual clock whenever a push button switch is pressed and released. The pressing of the button changes the Q and /Q outputs of the Flip- Flop and so positive going pulse and negative going pulse are generated. These can be tapped from 2mm terminals marked as High to Low Transition & Low to High Transition on the Digital Trainer Board.

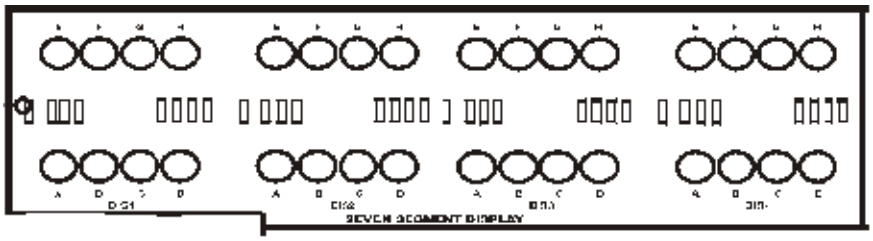


Logic Probe (Block-14)

The system use CMOS inverter IC CD4049 to sense logic LOW and logic HIGH. On reserving a pulse input both LED glow one by one but if the frequency is high then these two LEDs RED and GREEN appear to be glowing continuously. The logic probe can be used by inserting a probe lead in the 2mm terminal marked as logic input. The other end of the probe touched to a logic HIGH, the Red LED glows OR the probe is touched to logic LOW the Green LED glows. If the probe is touched to a pulse signal, the Red and Green LEDs flash if the frequency is low else both will appear to be glowing continuously.

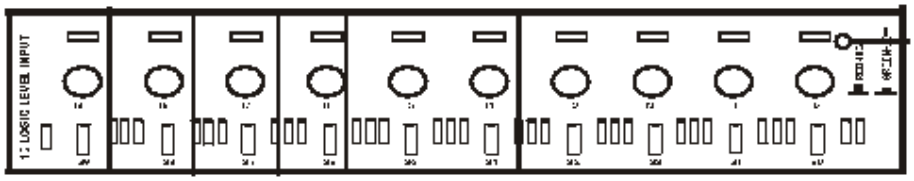
Seven Segment Display (Block-13)

The Digital Trainer provides Four Seven Segment displays on the board so that experiments involving displays can be conducted. The four seven segment display can be used as individual segment control.



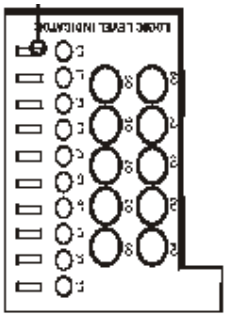
TTL/CMOS Logic Levels Input (Block-4)

The Digital Trainer has 10/16 Push Key Switch S0 to S9/S15 to generate ten TTL/CMOS input named as I0 to I9/I15 as marked on the Trainer Board. When the Switch is in Normal Mode, Logic Level High will generate & when the switch is in Push Mode, Logic Level Low will be generated on the 2mm banana socket provided on the kit. 10/16 Dual Color LEDs are used to indicate the logic input generated by each Push Key switch. The logic HIGH is indicated by the corresponding LED glowing as RED where the Logic LOW is indicated by the LED glowing as GREEN.



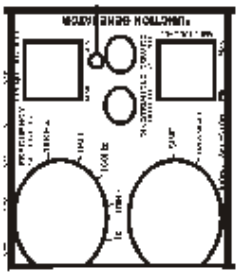
Logic Level Output Indicator (Block-1)

This Trainer has 10/16 Logic Level LED indicator for indicating output. The Logic high is indicated by LED glowing, where the logic low is indicated by LED is not glowing. Logic level output is given in 2mm banana socket provided on-board.



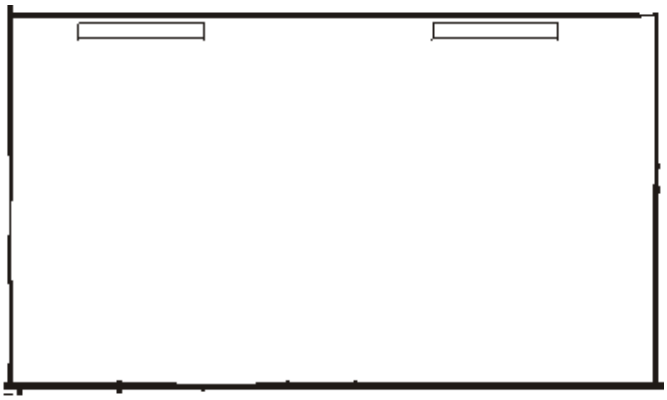
Function Generator (Block-2) for Analog Trainer

This Trainer has onboard Function Generator of up to 30 KHz Sine, Square & Triangle Frequency. Selector Switch is provided for five different frequency range selection of 1Hz, 10Hz, 100Hz, 1Khz & 10Khz. The Frequency of Sine, Square & Triangle can vary from the Frequency adjust pot. The Amplitude of sine & triangle can vary by Amplitude adjust pot. The Amplitude of Square wave output is fixed.



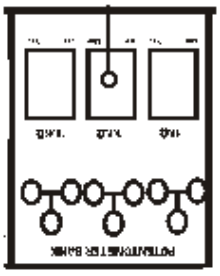
Bread Board Area (Block-5)

This Trainer provides a bread board area with 1200 TIE points in combination of 5 terminal strips TIE points and also provides 315 distribution points in combination of 10 terminal strip TIE points.



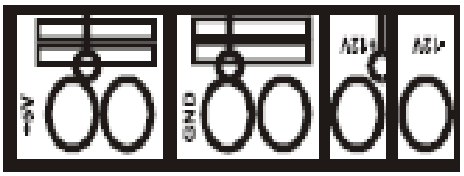
Variable Potentiometer (Block-3)

This Trainer provides on-board Variable Pot for 1K, 10K &100K for any digital/analog experiments.



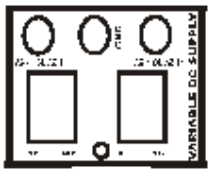
Fixed DC Supply (Block-6, 7, 8)

This Trainer provides on-board Fixed DC Power Supply of +5V/ 1A, GND, +12V/250mA, -12V/250mA. These Power terminals are provided in 2mm Banana Socket & 18 Pin Machine socket.



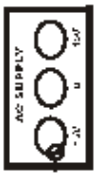
Variable DC Supply (Block-11) for Analog Trainer

This Trainer provides on-board Variable DC Power Supply from 0 to 15V/500mA & GND. These Power terminals are provided in 2mm Banana Socket. For varying the voltage POT is provided on-board.



AC Supply (Block-10) for Analog Trainer

This Trainer provides on-board AC Power Supply of 15V-0-15V. These Power terminals are provided in 2mm Banana Socket.



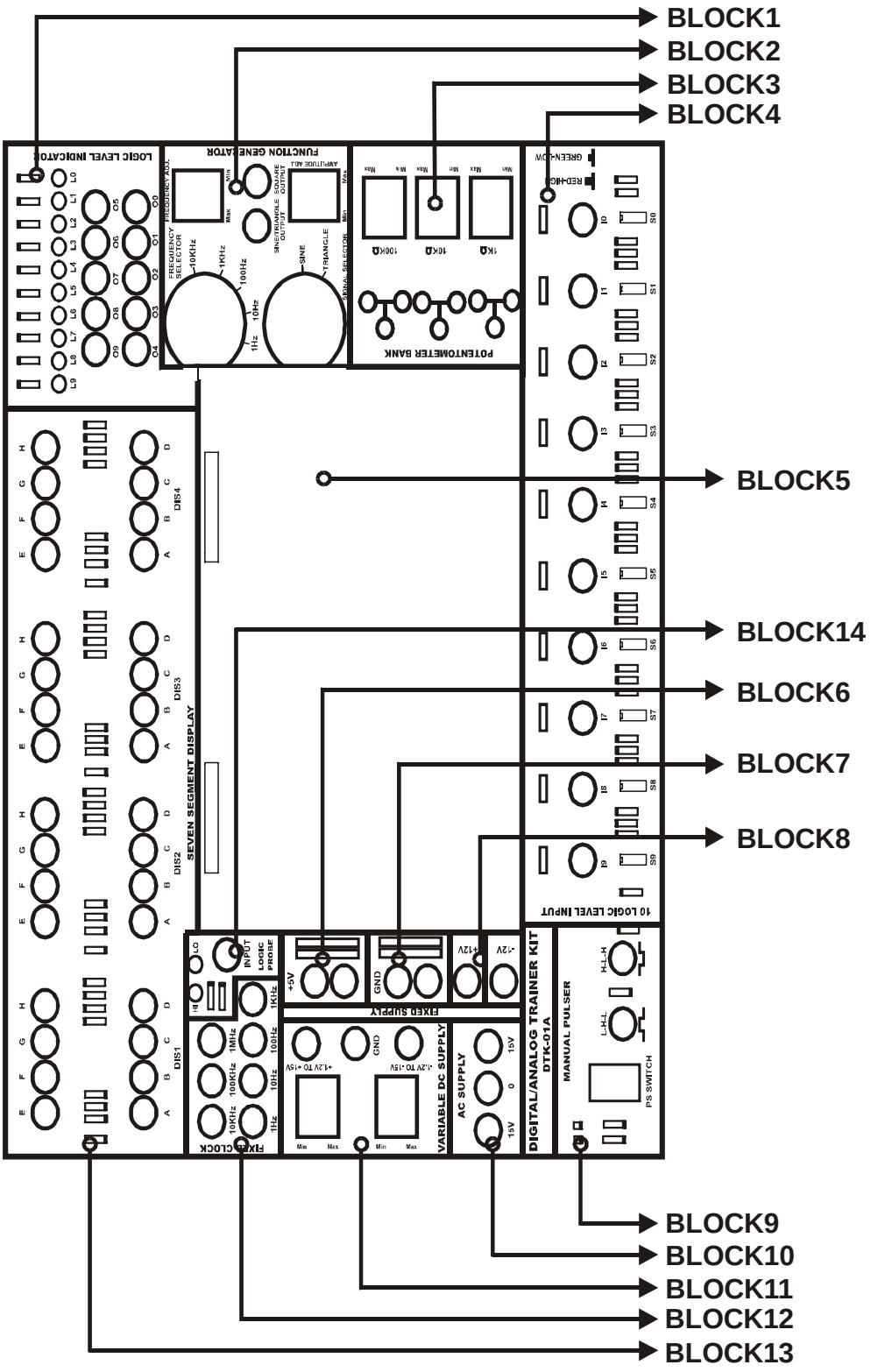
VOLTAGE PANEL METER for Analog Trainer

This Trainer provides on-board Voltage panel Meter to measure DC Voltage range from -20V to +20V.

20Pin ZIF Socket (Optional)

This Trainer provides on-board 20 Pin ZIF Socket to study function of any 8 pin to 20 pin IC's.

BLOCK DIAGRAM



HARDWARE INSTALLATION

The Digital/Analog Trainer Kit works on 230V, 50Hz power supply. By connecting 230V power point is by means of the power code of the Trainer. Please follow the below instruction while installing the Trainer.

1. Connect the Trainer kit to 230V power point.
2. Switch ON the power supply provided in the rear end of the kit.
3. Now your kit is ready for conducting the experiments on different ICs.

Note : Please take precaution to turn OFF the power supply while connecting the circuits.

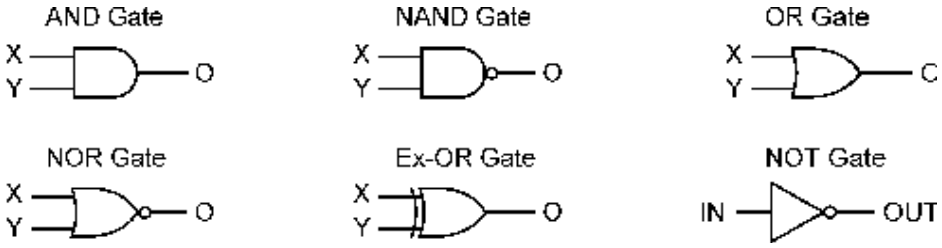
EXPERIMENT 1

Objective: Study of operation of all Logic Gates

Equipments Needed:

Components	**Quantity**
1. IC 7408 2 input AND Gate.	1
2. IC 7432 2 input OR Gate.	1
3. IC 7400 2 input NAND Gate.	1
4. IC 7402 2 input NOR Gate	1
5. IC 7486 2 input EX-OR Gate	1
6. IC 7404 NOT Gate.	1

Logic diagrams and IC Pin diagrams:



Truth Tables :

Input 1	Input 2	Output
X	Y	O
0	0	0
0	1	0
1	0	0
1	1	1

AND Gate

Input 1	Input 2	Output
X	Y	O
0	0	1
0	1	1
1	0	1
1	1	0

NAND Gate

Input 1	Input 2	Output
X	Y	O
0	0	0
0	1	1
1	0	1
1	1	1

OR Gate

Input 1	Input 2	Output
X	Y	O
0	0	1
0	1	0
1	0	0
1	1	0

NOR Gate

Input 1	Input 2	Output
X	Y	O
0	0	0
0	1	1
1	0	1
1	1	0

EX-OR Gate

Input	Output
0	1
1	0

NOT Gate

Procedure:

AND Gate:

1. Connect +5 V to pin no. 14 of IC 7408 and connect ground to pin no.7. (refer IC pin diagram)
2. Apply 0 (0 V) to pin no. 1 and 2 of IC 7408 shown in figure as per Truth Table.
3. Connect output of AND Gate i.e pin no.3 to input of logic probe or 10 bits LED display.
4. Switch on the instrument.
5. Observe output of Gate on 10 bits LED display.
6. Outputs can also be observed on oscilloscope.
7. Repeat steps 2, 3, 4 for different input combination.
8. Verify Truth Table.

NAND Gate :

1. Connect +5 V to pin no. 14 of IC 7400 and ground to pin no. 7.(Refer IC pin diagram)
2. Apply 0 (0 V) to pin no. 1 & 2 of IC 7400 shown in figure as per Truth Table.
3. Connect output of NAND Gate i.e. pin no.3 to input of logic probe or 10 bits LED display.
4. Switch on the instrument.
5. Observe output.
6. Repeat Step 2, 3, 4 for different input combinations.

OR Gate:

1. Connect +5 V to pin no. 14 of IC 7432 and connect ground to pin no.7 (Refer IC pin diagram)
2. Apply 0 (0V) to pin no. 1 and 2 of IC 7432 shown in figure as per Truth Table.
3. Connect output of OR Gate i.e pin no. 3 to input of logic probe or 10 bits LED display.
4. Repeat step 4, 5, 6 of NAND Gate.

NOR Gate :

1. Connect + 5V to pin no. 14 of IC 7402 and connect ground to pin no.7
2. Apply 0 (0V) to pin no. 2 and 3 of IC 7402 as per Truth Table.
3. Connect output of NOR Gate i.e. pin no. 1 to input of logic probe or 10 bits LED display.
4. Repeat step 4, 5, 6 of NAND Gate.

EX-OR Gate :

1. Connect +5V to pin no. 14 of IC 7486 and connect ground to pin no.7
2. Apply 0 (0V) to pin no. 1 and 2 of IC 7486 as per Truth Table.
3. Connect output of EX-OR Gate i.e pin no. 3 to input of logic probe or 10 bits LED display.
4. Repeat step 4, 5, 6 of NAND Gate.

NOT Gate :

1. Connect +5 V to pin 14 and ground to pin no.7 of IC 7404.
2. 0 (0V) to pin no. 1 of IC 7404 as per Truth Table.
3. Observe output on 10 bits LED display or Logic Probes

EXPERIMENT 2

Objective : Study of binary adders

A. Half Adder

B. Full Adder

C. Two Bit Binary Parallel Adder

A. Half Adder

Equipments Needed :

Components	**Quantity**
1. IC 7408 2 input AND Gate.	1
2. IC 7486 2 input EX-OR Gate.	1

Logic diagram :

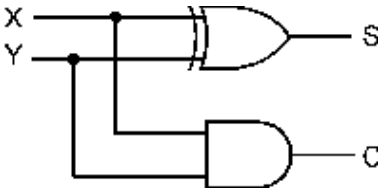


Figure 2

Truth Table :

Input1	Input2	Carry	Sum
X	Y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Procedure :

1. Make connections as shown in figure.
2. Connect +5V to pin no. 14 and ground to pin no.7 of IC 7408 and IC 7486. See IC Pin diagram.
3. Connect 0 (0V) to input x and y of adder shown as per Truth Table.
4. Switch ON the instrument.
5. Observe outputs S and C on 10 bits LED display.
6. Outputs can also be observed on oscilloscope.
7. Repeat steps 4,5,6,7 for other input combinations.
8. Verify Truth Table.

B. Full Adder:
Equipments Needed :

Component	**Quantity**
1. IC 7408 2 input AND Gate	1
2. IC 7432 2 input OR Gate	1
3. IC 7486 2 input EX-OR Gate	1

Logic diagram :

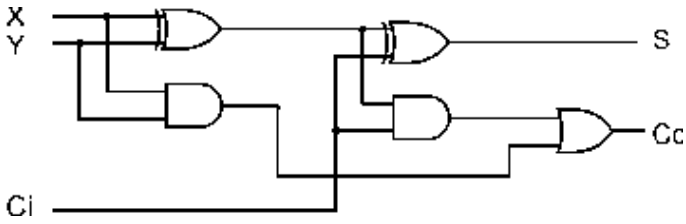


Figure 3

Truth Table :

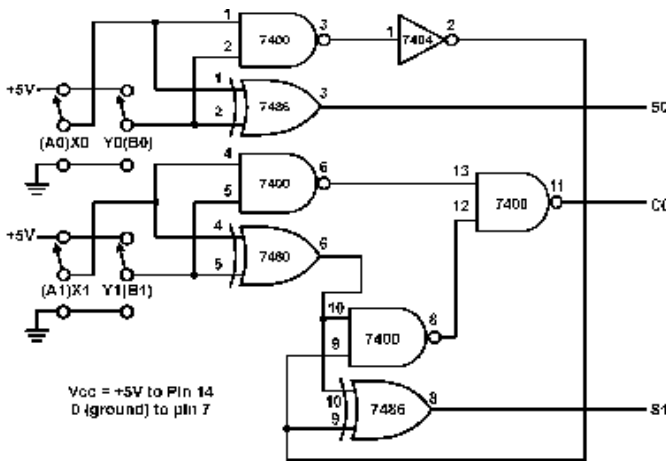
Input 1	**Input 2**	**Input Carry**	**Output Carry**	**Sum**
X	**Y**	**Ci**	**Co**	**S**
0	**0**	**0**	**0**	**0**
0	**0**	**1**	**0**	**1**
0	**1**	**0**	**0**	**1**
0	**1**	**1**	**1**	**0**
1	**0**	**0**	**0**	**1**
1	**0**	**1**	**1**	**0**
1	**1**	**0**	**1**	**0**
1	**1**	**1**	**1**	**1**

Procedure : Same as above

C. Two Bit Binary Parallel Adder
Equipments Needed :

Component	**Quantity**
1. IC 7400 2 input NAND Gate	1
2. IC 7486 2 input EX -OR Gate	1
3. IC 7404 Not Gate	1

Logic diagram :



Truth Table :

Sr. No.	Input 1 Bit 1	Input 2 Bit 2	Input 1 Bit 1	Input 2 Bit 2	Carry	Sum	Sum
	Al	**A0**	**B1**	**B0**	**C0**	**S1**	**S0**
1	0	0	0	1	0	0	1
2	0	1	0	1	0	1	0
3	0	1	1	1	1	0	0
4	1	0	1	0	1	0	0
5	1	0	1	1	1	0	1

Procedure :

1. Make connections as shown in figure.
2. Connect +5V to pin no. 14 and ground to pin no.7 of ICs.
3. See IC Pin diagram.
4. Connect 0 (0V) and 1 (+5 V) to inputs A1, A0, B1, B0 of adder shown as per truth table
5. Switch ON the instrument.
6. Observe outputs S1, S0 and C0 on 10 bits LED display.
7. Outputs can also be observed on oscilloscope.
8. Repeat steps 4, 6 for other input combinations.
9. Verify Truth Table.

Observation and Result:

Full adder can be implemented using two half Adder. Adders are studied and Truth Tables are verified.

EXPERIMENT 3

Objective : Study of Two Bit Binary Substractor (Half Subtractor)
Equipments Needed :

Component	**Quantity**
1. IC 7486 2 input EX-OR Gate.	1
2. IC 7408 2 input AND Gate	1
3. IC 7404 NOT Gate.	1

Logic diagram :

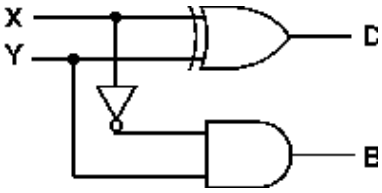


Figure 5

Truth Table :

Input 1	**Input 2**	**Borrow**	**Difference**
X	**Y**	**B**	**D**
0	0	0	0
0	1	1	1
1	0	0	1
1	1	0	0

Procedure :

1. Make connections as shown in figure.
2. Connect +5 V to pin no. 14 and ground to pin no.7 of ICs.
3. See Pin diagram.
4. Apply 0 (0V) to input x and y of subtractor shown as per Truth Table.
5. Switch ON the instrument
6. Observe outputs **B** and **D** on 10 bits LED display.
7. Outputs can also be observed on oscilloscope.
8. Repeat steps 4, 6, and 7 for other input combinations.
9. Verify Truth Table.

EXPERIMENT 4

Objective: Study of Binary to Gray Code Conversion
Equipments Needed:

Components	**Quantity**
1. IC 7486 2 input EX-OR Gate	2
2. IC 7404 NOT Gate	1

Logic diagram:

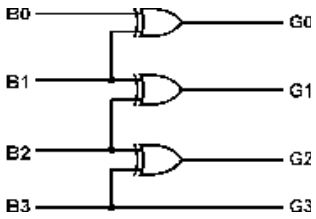


Figure 6

Truth Table :

Binary Code **Gray Code**

B3	B2	B1	B0	G3	G2	G1	G0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

Procedure :

1. Make connections as shown in figure.
2. Connect +5V to pin no. 14 and ground to pin no.7 of ICs.
3. See Pin diagram.
4. Apply 0 (0V) to binary inputs B3, B2, B 1, B0 shown as per Truth Table.
5. Switch ON the instrument
6. Observe outputs G3, G2, G1, G0 on 10 bits LED display.
7. Outputs can also be observed on oscilloscope.
8. Repeat steps 4, 6, 7 for other input combinations.
9. Verify Truth Table.

Result and Observation :

Binary to gray code conversion is studied. Most significant bit of binary as well as gray code is same as far as 4 bit code is concerned.

EXPERIMENT 5

Objective : Study Gray Code to Binary Code Conversions

Equipments Needed :

Component	**Quantity**
1. IC 7486 2 input EX-OR Gate	2

Logic Diagram :

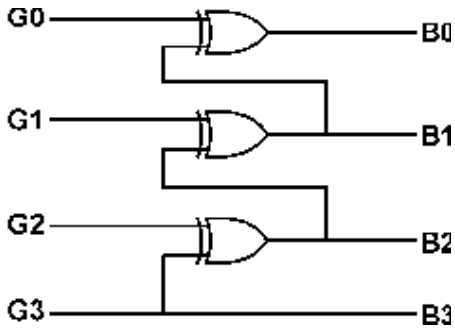


Figure 7

Truth Table :

Gray Code **Binary Code**

G3	G2	G1	G0	B3	B2	B1	B0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	1	0	0	1	0
0	0	1	0	0	0	1	1
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	1
0	1	0	1	0	1	1	0
0	1	0	0	0	1	1	1
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	1
1	1	1	1	1	0	1	0
1	1	1	0	1	0	1	1
1	0	1	0	1	1	0	0
1	0	1	1	1	1	0	1
1	0	0	1	1	1	1	0
1	0	0	0	1	1	1	1

Procedure :

1. Make connection as shown in figure (Refer pin diagram of IC)
2. Connect +5 V to pin no. 14 and ground to pin no. 7 of IC 7486.
3. Apply Gray code inputs G0, G 1, G2, G3 as per Truth Table.
4. Switch ON the instrument.
5. Observe outputs on 10 bits LED display.
6. Repeat above step for other input combinations.
7. Verify Truth Table.

EXPERIMENT 6

Objective : Study of Binary to Excess -3 Code Conversion

Equipments Needed :

Components	**Quantity**
1. IC 7432 2 input OR Gate.	1
2. IC 7408 2 input AND Gate	1
3. IC 7404 Not Gate	1

Logic diagram :

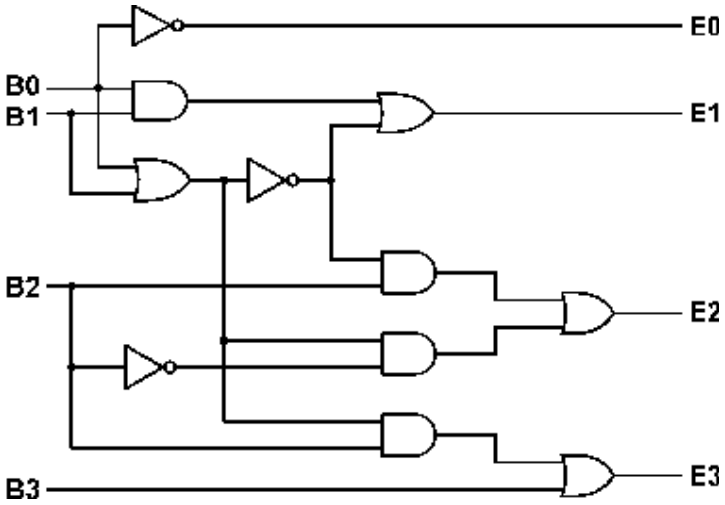


Figure 10

Procedure :

1. Make connection as shown in figure (Refer pin diagram of ICs)
2. Connect +5V to pin no. 14 and ground to pin no. 7 of ICs.
3. Connect 0 (0V) to binary inputs B3 B2 B1 B0 as per Truth Table.
4. Switch ON the instrument.
5. Observe outputs on 10 bits LED display.
6. Repeat steps 3, 5 for other input combinations.
7. Verify Truth Table.

Truth Table :

B3	B2	B1	B0	E3	E2	El	E0
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0
1	0	1	0	1	1	0	1
1	0	1	1	1	1	1	0
1	1	0	0	1	1	1	1

EXPERIMENT 7

Objective : Study of Characteristics of various types of Flip-Flops

Equipments Needed :

Component	**Quantity**
1. IC 7408 2 input AND Gate	2
2. IC 7432 2 input OR Gate	1
3. IC 7400 2 input NAND Gate	1
4. IC 7402 2 input NOR Gate	1

Logic diagram :

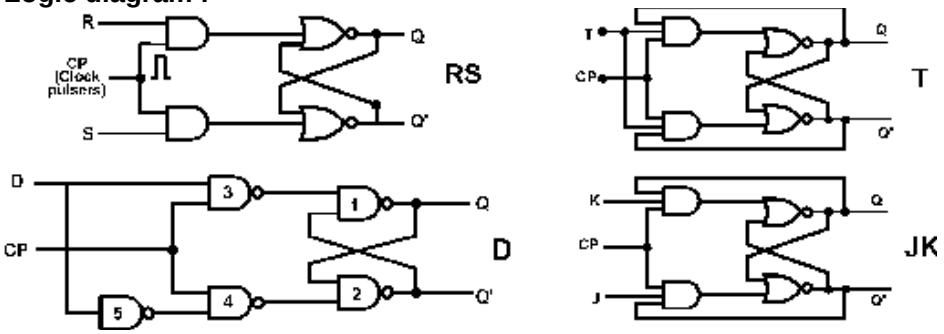


Figure 9

Truth Table :

Clocked RS **Flip Flop JK flip flop**

Present state	**Input 1**	**Input 2**	**Next State**	**Present state**	**Input**	**Input**	**Next State**
Q	**S**	**R**	**Q(t +1)**	**Q**	**J**	**K**	**Q (t+ 1)**
0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0
0	1	0	1	0	1	0	1
0	1	1	In determinant	0	1	1	1
1	0	0	1	1	0	0	1
1	0	1	0	1	0	1	0
1	1	0	1	1	1	0	1
1	1	1	In determinant	1	1	1	0

Present state	Input	Next state
Q	**T**	**Q (t+ 1)**
0	0	0
0	1	1
1	0	1
1	1	0

T Flip Flop

Present state	Input	Next state
Q	**D**	**Q (t +l)**
0	0	0
0	1	1
1	0	0
1	1	1

D Flip Flop

Procedure :

1. Make connections as shown in figure for each flip-flop one by one. (Refer pin diagram of ICs)
2. Connect +5 V to pin no. 14 and ground to pin no. 7 of ICs.
3. Connect pulsar switch output (Y) to clock input CP of flip-flop
4. Connect input l or 0 to inputs of flip-flops as per Truth Table shown.
5. Switch ON the instrument.
6. Press pulsar switch to get output.
7. Observe outputs on 10 bits LED display or logic probe.
8. Repeat above steps 4, 5, 6 for other input combinations.
9. Verify Truth Tables.

Observations :

1. Indeterminate state of RS flip-flop is determined in JK flip-flop.
2. Toggle state in JK flip-flop is eliminated in master slave flip-flop.

EXPERIMENT 8

Objective : Study of Crystal Oscillator

Equipments Needed :

Components	**Quantity**
1. Resistance 330R	3
2. Crystal 1 MHz	1
3. Capacitor	
0.01 μFD	1
100 PF	1
4. IC 7404 Hex Inverter	1

Logic diagram :

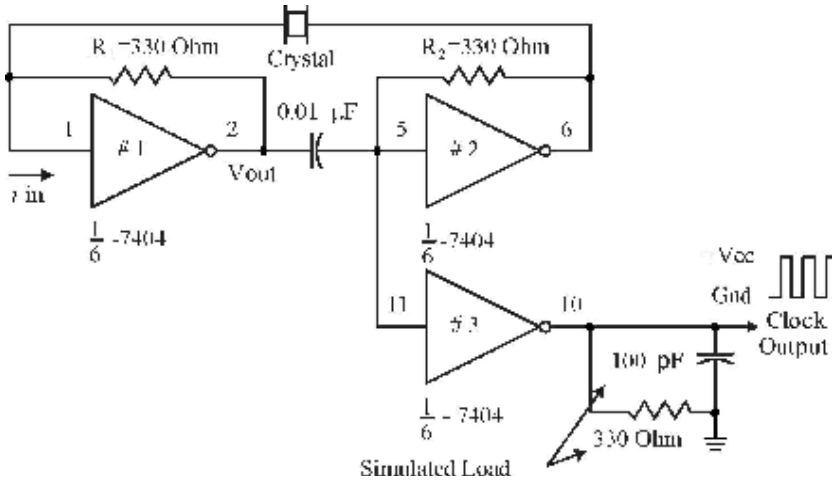


Figure 10

Procedure :

1. Make connections as shown in figure (Refer pin diagram of ICs)
2. Connect +5V to pin no. 14 and connect ground to pin no. 7 of IC 7404.
3. Switch ON the instrument.
4. Observe oscillator output on oscilloscope.
5. Measure the frequency.
6. Compare with frequency of crystal.

Observation and Result:

Crystal oscillator frequency depends solely on crystal dimensions and independent of any other parameter.

EXPERIMENT 9

Objective : Study of 4 bit Binary up down Counter

Equipments Needed :

Components	**Quantity**
1. IC 74107 Dual JK flip flop with clear	2
2. IC 7408 2 input AND Gate	2
3. IC 7432 2 input OR Gate.	1

Logic diagram :

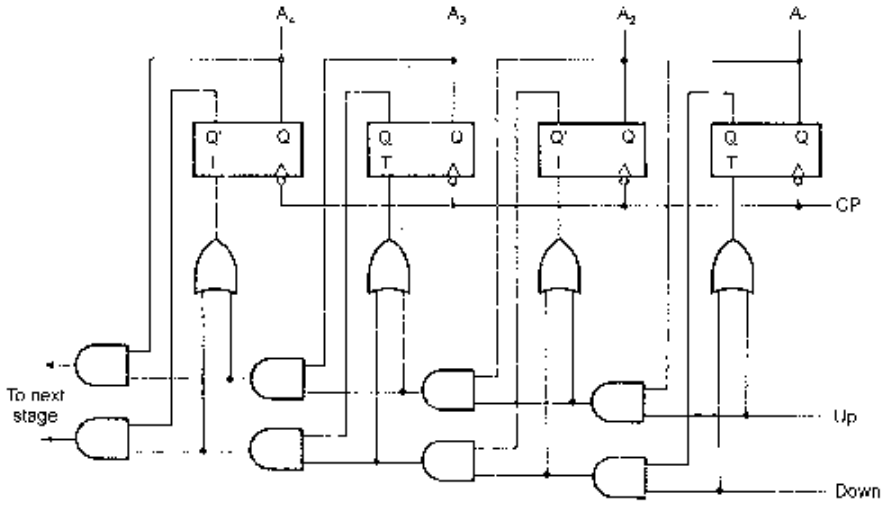


Figure 11

Procedure :

1. Make connection as shown in figure (Refer pin diagram of ICs)
2. Connect +5V to pin no.14 and ground to pin no. 7of ICs.
3. Connect +5V to the UP terminal of Counter and ground to DOWN terminal.
4. Connect ground to clear input of flip flop.
5. Disconnect ground from clear input of flip flop.
6. Connect Y output of pulsar switch to clock input of flip-flop.
7. Switch ON the instrument.
8. Press pulsar switch.
9. Observe outputs on 10 bits LED display.
10. Press pulsar switch 12 times and observe change in output. It will follow Sequence as shown in Truth Table for UP counter.
11. Connect + 5V to DOWN terminal and ground to UP terminal.
12. Repeat steps 6, 7, and 10 for counter to count down.
13. Verify Truth Table.

Truth Table :

Up Counter

A4	A3	A2	A1
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

Down Counter

A4	A3	A2	Al
1	1	1	1
1	1	1	0
1	1	0	1
1	1	0	0
1	0	1	1
1	0	1	0
1	0	0	1
1	0	0	0
0	1	1	1
0	1	1	0
0	1	0	1
0	1	0	0
0	0	1	1
0	0	1	0
0	0	0	1
0	0	0	0

EXPERIMENT 10

Objective : Study of Johnson Counter
Equipments Needed :

Components	**Quantity**
1. IC 7474 D flip flop	2
2. IC 7408 2 input AND Gate	2

Logic diagram:

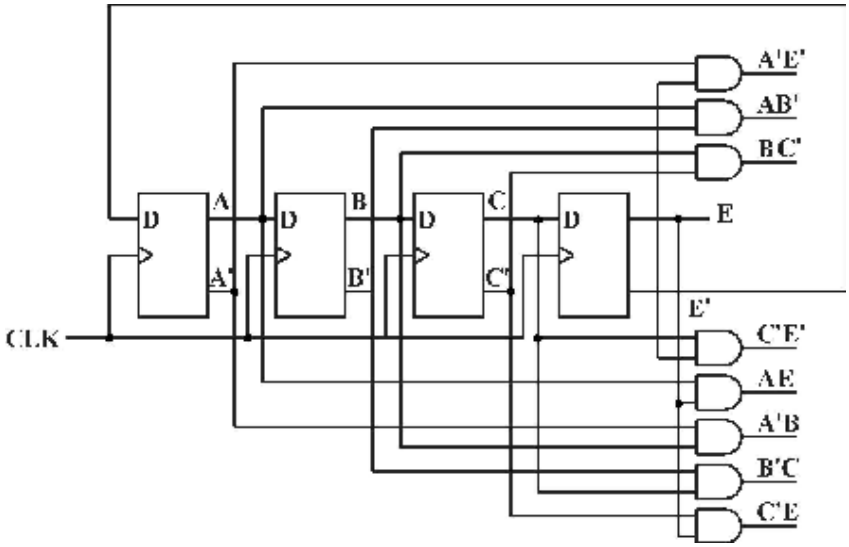


Figure 12

Truth Table :

Sr. No.	Flip flop output A	B	C	E	AND Gate required for output
1	0	0	0	0	A'E'
2	1	0	0	0	AB'
3	1	1	0	0	BC'
4	1	1	1	0	CE'
5	1	1	1	1	AE
6	0	1	1	1	A'B
7	0	0	1	1	B'C
10	0	0	0	1	C'E

Procedure :

1. Make connections as shown in figure (Refer to pin diagram of ICs)
2. Connect +5 V to pin no. 14 and ground to pin no. 7of ICs.
3. Connect ground to clear input of flip flop and disconnect it.
4. Connect A output of pulsar switch to clock input of flip-flops.
5. Switch ON the instrument.
6. Press pulsar switch.
7. Observe outputs on 10 bits LED display.
8. Press pulsar switch 7 times and observe change in output. It will follow Sequence as shown in Truth Table.
9. Verify Truth Table.
10. AND & NOT Gates can be used to make product terms of last column and can be observed on 10 bits LED display to know when a particular Combination occurs.

Result :

Johnson counter gives 2k distinguishable states with k flip-flop.

EXPERIMENT 11

Objective : Study of 4 Bit Serial in Parallel out Shift Register
Equipments Needed :

Components	**Quantity**
1. IC 7474 D flip flop	1

Logic diagram :

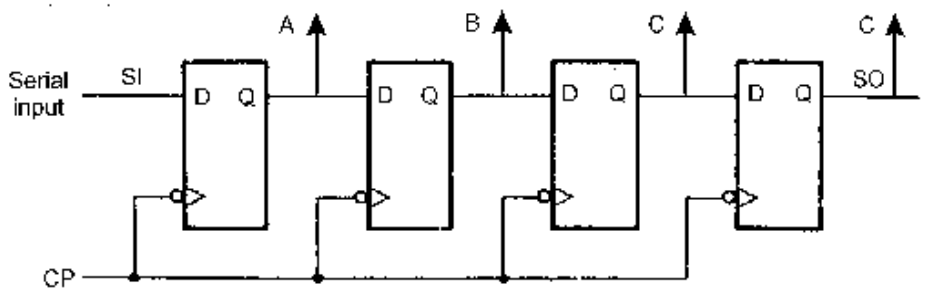


Figure 13

Truth Table :

A	B	C	D
0	0	0	0
1	0	0	0
1	1	0	0
1	1	1	0
1	1	1	1

Procedure :

1. Make connections as shown in figure (Refer to pin diagram of ICs)
2. Connect +5V to pin no. 14 and ground to pin no. 7 of IC 7474.
3. Switch ON the instrument.
4. Clear all flip-flops by applying ground to clear input of flip-flops.
5. Apply +5V to serial input SI of shift register.
6. Connect A output of pulsar switches to clock input of flip-flops.
7. Trigger flip-flops four times by pressing pulsar switch 4 times.
8. Observe output of each flip-flop on 10 bits LED display. It will be as indicated in table.
9. As shown in table, 1 is shifted to right each time flip-flop is triggered.

EXPERIMENT 12

Objective: Study of 10 to 3 Line Encoder
Equipments Needed:

Component	**Quantity**
1. IC 7432 2 input OR Gate	2

Logic diagram:

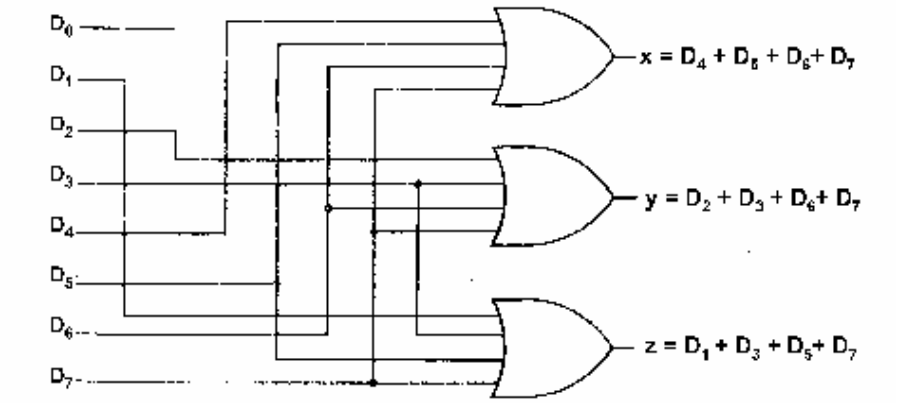


Figure 14

Truth Table :

D0	D1	D2	D3	D4	D5	D6	D7	x	y	z
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

Procedure :

(Use two 2 input OR Gate in place of one 4 input OR Gate.)
1. Make connections as shown in figure (Refer to pin diagram of ICs)
2. Connect +5 V to pin no. 14 and ground to pin no. 7 of IC 7432.
3. Connect input 1(+5V) or 0 (0V) to encoder circuit as shown in figure as per truth table.
4. Switch ON the instrument.
5. Observe outputs on 10 bits LED display.
6. Repeat step no. 3 and 5 for other input combination.
7. Verify Truth Table.

EXPERIMENT 13

Objective :
Study of 3 to 10 Line Decoder
Equipments Needed :

Components	**Quantity**
1. IC 7411 3 input AND Gate.	3
2. IC 7404 Inverter.	1

Logic diagram :

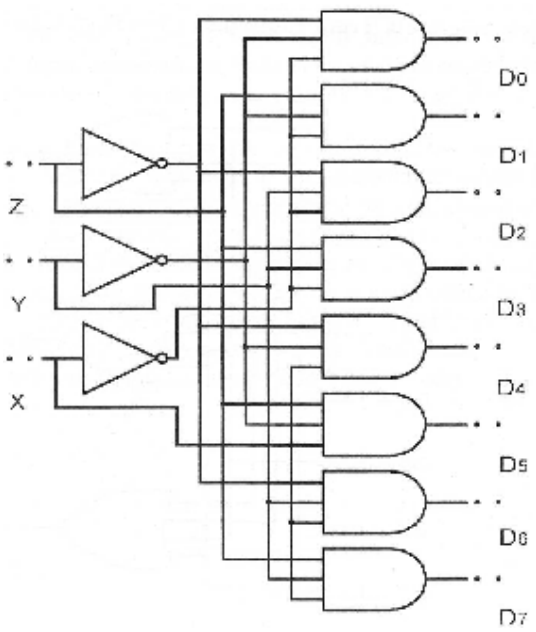


Figure 12

Truth Table :

x	y	z	D0	Dl	D2	D3	D4	D5	D6	D7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	1	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

Procedure :

1. Make connections as shown in figure (Refer to pin diagram of ICs)
2. Connect +5 V to pin no. 14 and ground to pin no. 7 of IC 7404 and IC 7411.
3. Connect input 1 or zero to decoder circuit as shown in figure as per Truth Table.
4. Switch ON the instrument.
5. Observe outputs on 10 bits LED display.
6. Repeat step no. 3 and 5 for other inputs.
7. Verify Truth Table.

EXPERIMENT 14

Objective : Study of Multiplexer and De-multiplexer Circuit

Equipments Needed :

Component	**Quantity**
1. IC 7411 3 input AND Gate.	2
2. IC 7432 2 Input OR Gate.	1
3. IC 7404 NOT Gate.	1

Logic diagram:

4 To 1 Line Multiplexer

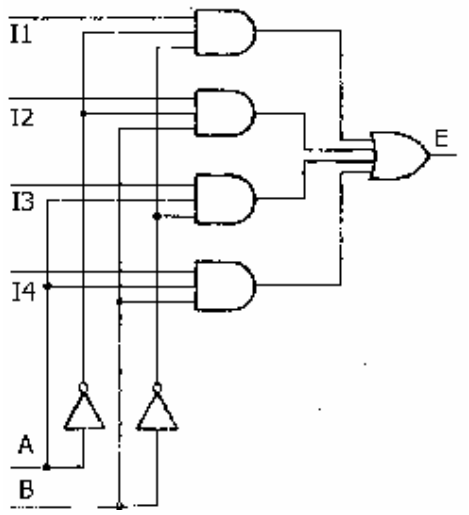


Figure 16

Truth Table:

Selection line 1 (A)	**Selection line 2 (B)**	**Input Selected (E)**
0	0	I 1
0	1	I 2
1	0	I 3
1	1	I 4

Procedure :

1. Make connections as shown in figure (Refer pin diagram of ICs).
2. Connect + 5 V to pin no. 14 and ground to pin no.7 of ICs.
3. Apply inputs 1 or 0 to input lines 11, 12, 13, 14.
4. Connect 0 to selection lines S1 and S0 as shown in Truth Table.
5. Switch ON the power supply.
6. Observe outputs on 10 bits LED display or logic probe.
7. If input applied is square wave or pulse then CRO can be used to view Waveforms at output.
8. Repeat step 4 for other input combination.
9. Follow above steps and prove Truth Table.

Equipments Needed :

Component	**Quantity**
1. IC 7404 NOT Gate	1
2. IC 7410 NAND Gate	2

Logic diagram :

1 To 4 Line De-multiplexer :

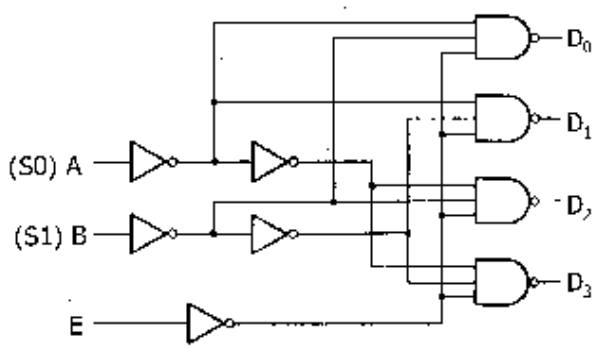


Figure 17

Truth Table :

Input	**Selection line**	**Selection line**	**Output Line**	**Output Line**	**Output Line**	**Output Line**
E	**S0**	**S1**	**D0**	**Dl**	**D2**	**D3**
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

Procedure :

1. Make connections as shown in figure (Refer pin diagram of ICs).
2. Connect + 5 V to pin no. 14 and ground to pin no.7 of ICs.
3. Apply inputs 1 or 0 to input E.
4. Connect 0 to selection lines S1 and S0 as shown in Truth Table.
5. Switch ON the instrument
6. Observe outputs on 10 bits LED display or logic probe.
7. If input applied is square wave or pulse then CRO can be used to view waveforms at output.
8. Repeat step 4 & 6 for other input combinations.
9. Follow above steps and prove Truth Table.

EXPERIMENT 15

Objective: Study of Pulse Stretcher Circuit

Equipments Needed :

Components	**Quantity**
1. IC 7400 2 input NAND Gate	1
2. Capacitors 0.01 MF	1
0.022 MF	1
0.033 MF	1
3. Resistance 5600 Ω	2

Logic diagram:

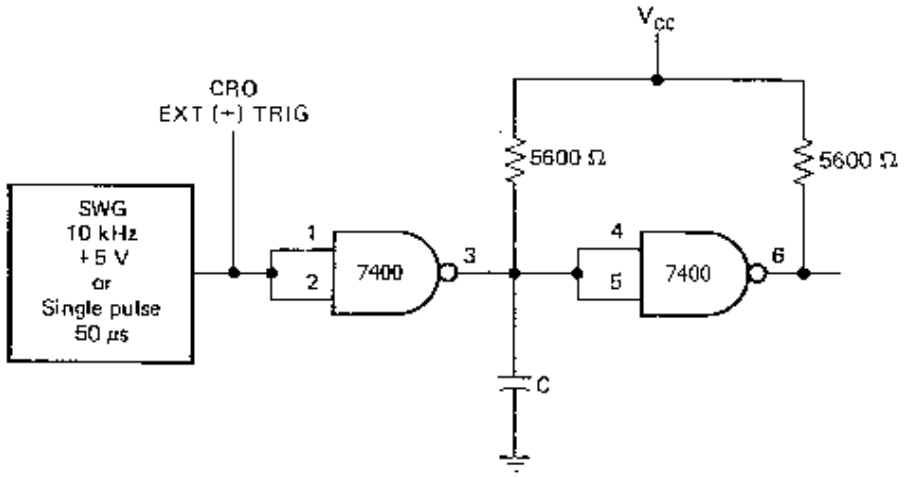


Figure 110

Procedure:

1. Make connections as shown in figure (Refer pin diagram of ICs)
2. Select clock generator at 10 KHz & Connect
Clock generator output to the terminal marked input.
3. Switch ON the Instrument.
4. Apply same pulse to ext trigger input of CRO for triggering time base.
5. See the output waveform on CRO.
6. Change value of capacitor C and observe the change in width.
7. Follow the above steps and complete table shown.

Observation :

Sr. No.	Capacitance	Pulse width at terminal 6
1	0 MF	
2	0.001 MF	
3	0.022 MF	
4	0.033 MF	

Result:
The width of output at point 3 is longer than that at A because it takes capacitor C time to charges up to the threshold voltage of Gate 2.

EXPERIMENT 16

Objective :

Study of method of Interfacing CMOS Logic family with TTL Logic family

Introduction :

The CMOS logic family can be operated at the same power supply voltage as TTL but with a sacrifice in speed. To operate the CMOS family at its maximum speed requires operation with Vdd equal to 12V. To interface with TTL requires a level shifting device. CMOS logic elements can easily drive other CMOS elements because of their high input resistance. However, most CMOS logic elements cannot provide the current required by a single load of the medium-power TTL series. To satisfy this current requirement requires high current CMOS buffer element.

Equipments Needed :

Component	**Quantity**
1. IC 7406 NOT Gate	1
2. IC 4001 NOR Gate	1
3. IC 4050 CMOS Buffer	1

Logic diagram:

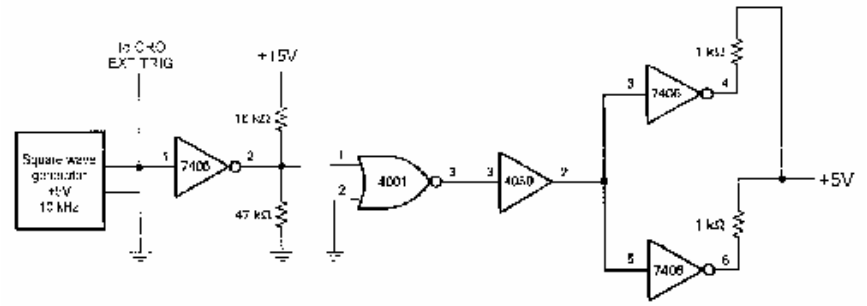


Figure 19

7406 Vcc = +5 volts to pin 14
0 (ground) to pin 7
4001 VDD = + 12 volts to pin 14
Vss = 0 (ground) to pin 7
4050 Vcc = + 5 volts to pin 1 (note pin number)
Vss = 0 (ground) to pin 10

Procedure :

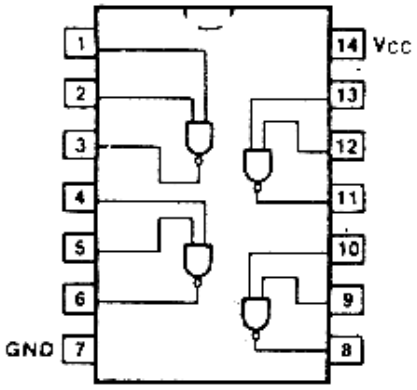
1. Make connections as shown in figure (Refer pin diagram of ICs)
2. Connect +5 V to pin no. 14 and ground to pin no. 7 of IC 7406.
3. Connect + 12 V to pin no. 14 and ground to pin no. 7 of IC 4001.
4. Connect +5 V to pin no. 1 and ground to pin no. 10 of IC 4050.
5. View and sketch the waveform at
   a. 4001 pin 1
   b. 4001 pin 3
   c. 4050 pin 2
   d. 7406 pin 4

Result:

CMOS to TTL interface circuit is studied.

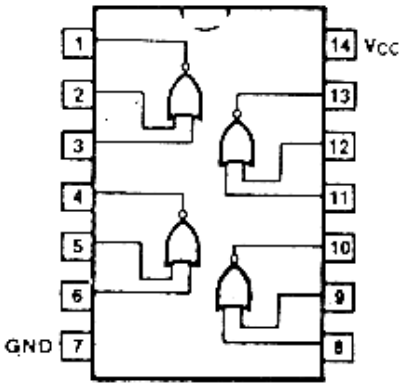
PIN DIAGRAMS OF ICS

54/7400
54H/74H00
54S/74S00
54LS/74LS00
QUAD 2-INPUT NAND GATE

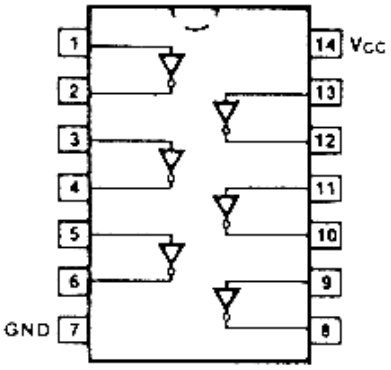


54/7402
54S/74S02
54LS/74LS02

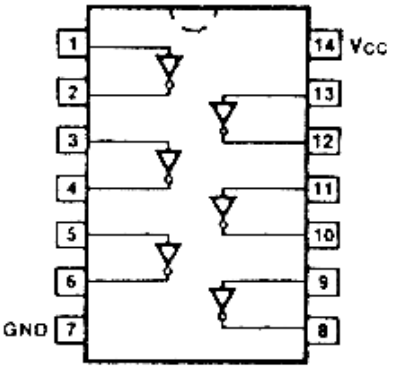
QUAD 2-INPUT NOR GATE



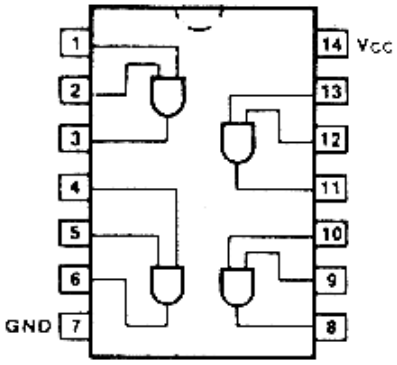
54/7404
54H/74H04
54S/74S04
54S/74S04
54LS/74LS04
HEX INVERTER



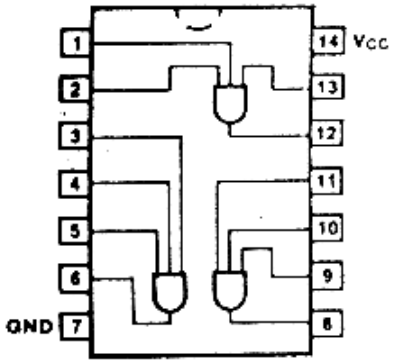
54/7406
HEX INVERTER BUFFER/ DRIVER
(WITH OPEN-COLLECTOR
A HIGH- VOLTAGE OUTPUT)



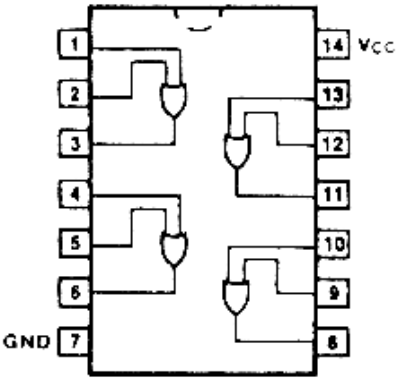
54/7408
54H/74H08
54S/74S08
54LS/74LS08
QUAD 2-INPUT AND GATE



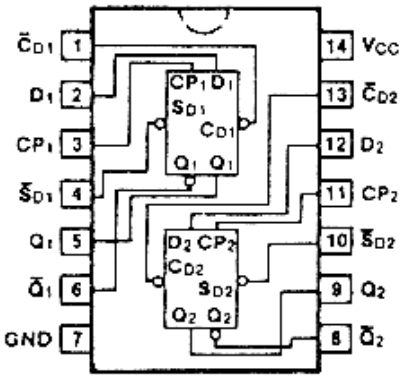
54/7411
54H/74H11
54S/74S11
54LS/74LS11
TRIPLE 3-INPUT AND GATE



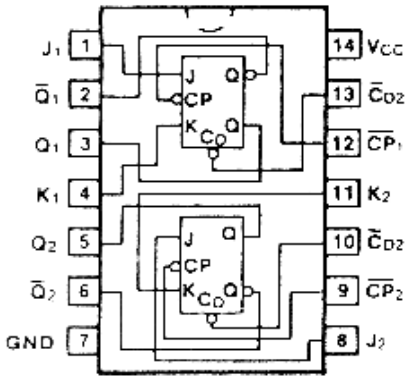
4/7432
4S/74S32
4LS/74LS32
AD 2-INPUT OR GATE



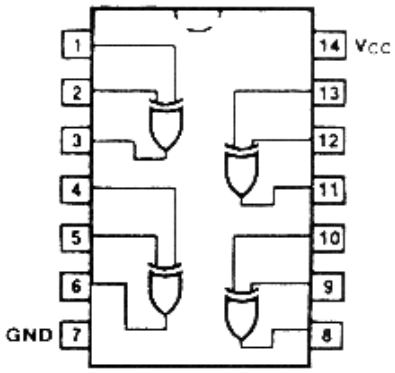
54/7474
54H/74H74
54S/74S7
54LS/74LS74
DUAL D-TYPE POSITIVE
EDGE TRIGGERED FLIP FLOP



54/74107
54LS/74LS107
DUAL JK FLIP FLOP
(WITH SEPARATE
CLEARSAND CLOCKS)



54LS/74LS86
QUAL 2-INPUT EXCLUSIVE OR GATE



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