AKADEMIKA

DCL-05

DATA CONDITIONING AND RECONDITIONING KIT

EXPERIMENTAL MANUAL

…. A MESSAGE FROM

AKADEMIKA

Today's system designers are faced with tomorrow's problems. DIGITAL COMMUNICATION is one of the important subject need to teach while learning electronics.
It is our vision to provide you with the product you need for training ensuring lasting reliability & quality.

OUR MOTTO:

- Light years ahead – refers to leadership.

As leaders in our industry in India, we are totally committed to servicing as the standard against which all are measured in the areas of

• Design • Quality • Value • Delivery • Support.

We are truly light years ahead of our competition in this area. That means that you our valued customers are guaranteed satisfaction.

As you will move through this manual you will quickly discover that we have complete, truly innovative &superior training products. We are so committed to quality that we back our products with a complete comprehensive warranty.

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SAFETY RULES

Carefully follow the instructions contained in this manual as they provide you with important points on safety during the installation, use and maintenance. Keep this manual always with you for easy reference.

Arrange all accessories in order after unpacking, so that its integrity is checked with respect to its checklist. Also ensure that no visible damage as such appear on any accessories.

Before connecting the power supply to the kit, be sure that the jumpers and connecting chords are connected correctly as per experiment.

In DCL-05kit, signals are to be monitored with an oscilloscope as explained in the manual. For observation of signals on oscilloscope either use X10(Attenuation Probe) or 180Ω resistance in series with normal oscilloscope probe.

These kits must be employed only for the use for which it has been conceived, i.e.as educational equipment, and must be used under the direct survey of expert personnel. Any other use is improper and so dangerous. The manufacturer cannot be considered responsible for eventual damages due to improper, wrong or unreasonable uses.

In case of any fault or malfunctioning in the trainer kit, turn off the power supply and do not tamper the kit. In case servicing is required, contact the service center for technical assistance.

The kits are liable to malfunction/under-perform if they are not operated under following conditions,

- Ambient temperature: from 0 to 45 ° C.
- Relative humidity: from 20 to 80 %.

Avoid any immediate/significant change of temperature and humidity.

WARRANTY

These kits are warranted against defects in workmanship and materials. Any failure due to defect in either workmanship or material should occur under normal use within a year from the original date of purchase, such failure will be corrected free of charge to the purchaser by repair or replacement of defective part or parts. When the failure is result of user's neglect, natural disaster or accident, we charge for repairs regardless of the warranty period. The warranty does not cover perishable items like connecting chords, Crystals, etc. and other imported items.

This warranty is subject to the following conditions and limitations. The warranty is void and inapplicable if the defective product is not brought or sent to our authorized service center or sales outlet within the warranty period. Defective product is, on Falcon Electro - Tek Pvt. Ltd's sole judgment. The defective product will be replaced with new one or repaired without charge or with charge.

In the warranty period if the service is needed, purchaser should get in touch with the service center or sales outlet. The purchaser should return the product to the service center or sales outlet at his or her sole expense. The loss and damage in transit will be outside the preview of this warranty. A returned product must be accompanied by a written description of the defects. Type and Model No. of kits has to be mentioned specifically. We return the product to the purchaser at our expense. In case that warranty does not cover the product on Falcon Electro-Tek Pvt. Ltd.'s judgment, we repair the product after obtaining prior permission from purchaser who receives an estimate statement about repairing charges. In such case, Falcon Electro-Tek Pvt. Ltd. bares the transporting expenses required to send back all the repaired products for the moment, and then repairs and transporting expenses will be charged against the purchaser by the statement of accounts.

When the authorized sales agents sell our products, they must notify the purchaser of the warranty contents, but have no rights to stretch the meaning of original warranty contents or offer additional warranty. Falcon Electro-Tek Pvt. Ltd. does not provide any other promise or suggestive warranty and hold no liability for the damage caused by negligence, abnormal use or natural disaster. Falcon Electro-Tek Pvt. Ltd. is not responsible for the damages even if it is notified of above dangers in advance as well.

For more special service or overall repairs, maintenance and upgradation of products, be sure to contact our service center or sales outlet.

INDEX

TECHNICAL SPECIFICATIONS

DCL-05: DATA CONDITIONING AND RECONDITIONING KIT.

DATA SIMULATOR **:** Onboard 8-bit variable NRZ-L pattern.

CRYSTAL OSCILLATOR **:** 6.40 MHz

DATA CLOCK **:** 266 KHz.

DATA ENCODING **:**NRZ-L NRZ-M, NRZ-S, URZ, BIO-L, BIO-M, BIO-S, Unipolar to Bipolar, AMI.

DATA DECODING **:** NRZ-L NRZ-M, NRZ-S, URZ, BIO-L,BIO-M, BIO-S, Bipolar to Unipolar, AMI.

INTER CONNECTION **:** 2 mm banana socket.

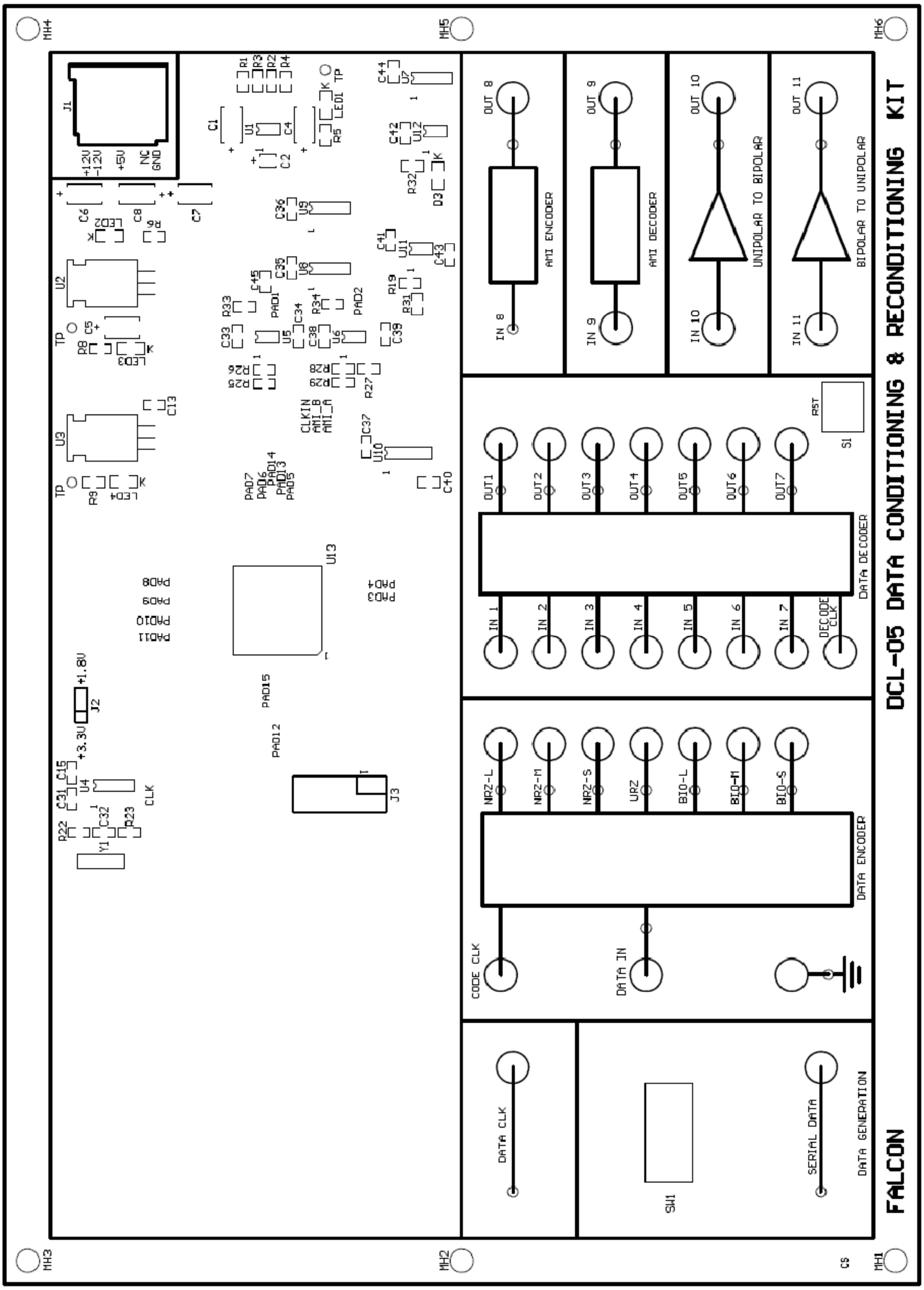
POWER SUPPLY **:** -12V, +5V, GND.

TEST POINTS **:** 26.

ACCESSORIES

	DCL -05	Quantity
1	Short Links PCS2 Patch cord Male To Male	2
2	Mini Link Patch cords Male To Male	12
3	DCL-05 EXPT Manual	1
4	Power Supply (DCS)	1
5	Power cord	1

FUNCTIONAL BLOCK



INTRODUCTION

AKADEMIKA with the trainer, namely, "DCL-05initiates the user to the various Data Conditioning and Reconditioning Techniques, normally adopted in practice.

"DCL-05": DATA CONDITIONING AND RECONDITIONINGKIT.

FEATURES:

1) The System illustrates the use of the following data formats:
   a) Non Return to Zero - Level (NRZ-L)
   b) Non Return to Zero - Mark (NRZ-M)
   c) Non Return to Zero - Space (NRZ-S)
   d) Unipolar Return to Zero (URZ)
   e) Biphase - Level (Biphase-L)
   f) Biphase - Mark (Biphase-M)
   g) Biphase - Space (Biphase-S)
   h) Alternate Mark Inversion (AMI)
   i) Unipolar To Bipolar

2) The trainer comes with an onboard data simulator, which generates the NRZ-L pattern depending on positions of 8-bit switch and the reference clock (266 KHz), which enables the trainers to work in a stand-alone mode.

3) Interconnection facilities:
   Sockets and patch chords are provided for on board connections.

4) Test Points:
   All relevant test points are brought-out for observations. Observations are carried out on an oscilloscope.

5) Power Supply:
   -12V, +5V, GND.

PRINCIPLE OF DATA CONDITIONING

The Digital data in the systems can be encoded in several formats. All these waveforms can be broadly classified into the following four groups:

1. Non-return to Zero formats,
2. Return to Zero formats,
3. Phase encoded formats,
4. Multilevel binary formats.

It is common that some puzzling questions may arise to a beginner as to why there should be so many PCM Waveforms? And are there really so many unique applications necessitating such a variety of waveforms to represent the “ones” and “zeros”? The reason for the large selection relates to the difference in performances that characterize each waveform. In choosing a coding scheme for a particular application, the common parameters worth examination are as follows:

1) DC Component:
The DC component associated with the data formats has to be minimized, if the system is to be AC coupled. The proper selection of the data format ensures optimum DC component that is associated with the signal power spectrum.

2) Self Clocking:
The presence of sufficient number of transition in the transmitted data enables the receiver to derive the clock from the data. Thus it is preferable to select a data format, which enables sufficient number of transitions in the transmitted data stream. For example, the biphase signals allow sufficient number of transitions in the transmitted data, compared to the corresponding Non-return to zero signals.

3) Band Width:
The proper selection of the coding enables to optimize the bandwidth requirement.

4) Noise Immunity:
The various PCM Waveform types can be further characterized by the probability of bit error versus signal to noise ratio. For Example, the NRZ waveforms have better immunity to noise than the corresponding unipolar return to zero signal, which enables an error free transmission.

Circuit Description

- **Clock And Data Generator**

This block generates NRZ-L data of a variable pattern depending on positions of eight bit switch SW1 also Reference clock of frequency 266KHz (DATA CLK) is generated. Serial Data and Data clock is generated by programming the CPLD (Complex Programmable Logic Devices) i.e. IC U13 (LC4128ZE-7TN144C).This is achieved by using Parallel to Serial Shift Register. Clock to the CPLD is fed by the crystal which gives6.4MHz clock.

- **Data Encoder and Decoder**

The NRZ-L, NRZ-M, NRZ-S, URZ, BIO-L, BIO-M, BIO-S data encoding and decoding is done by programming the CPLD.

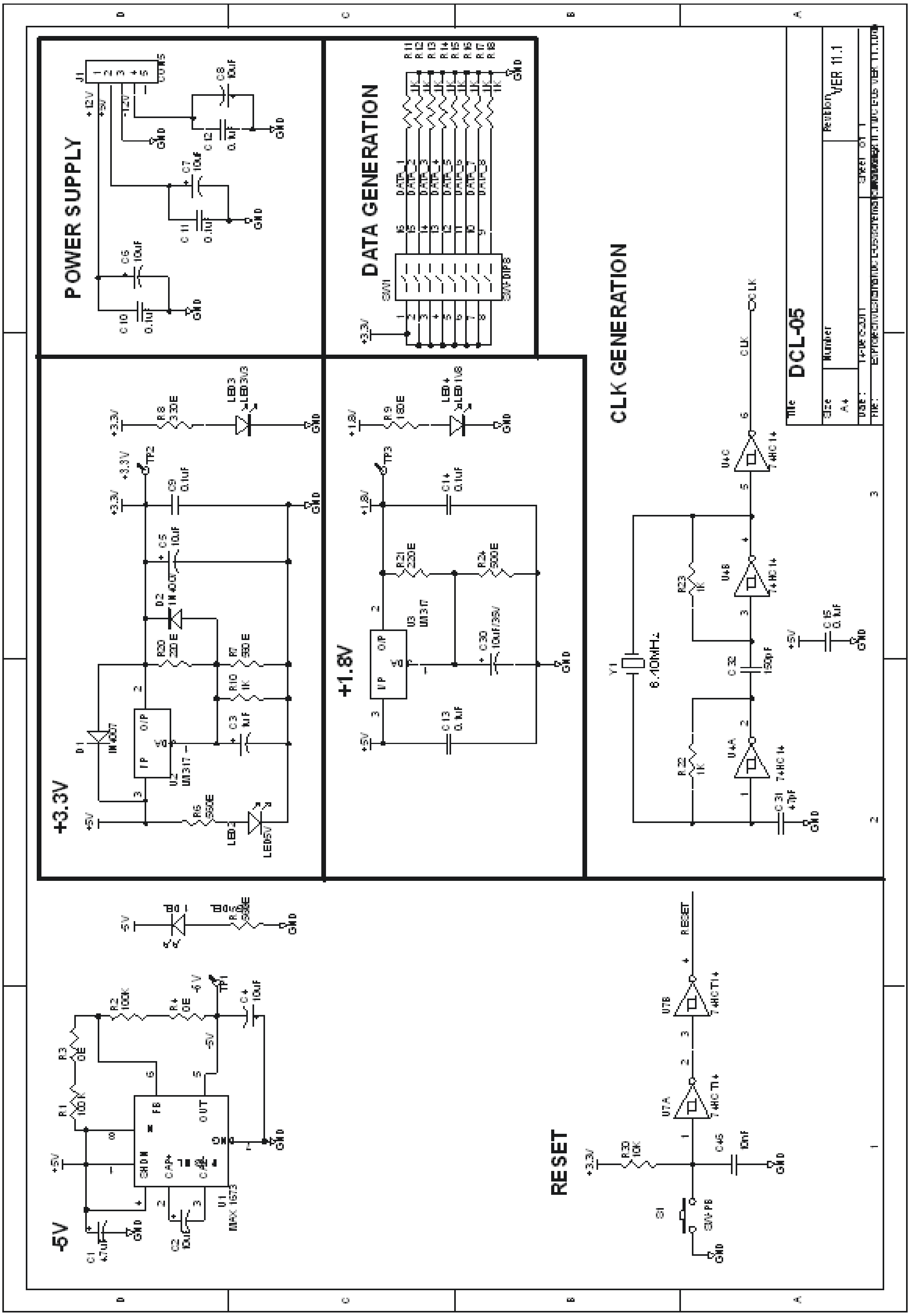
- **AMI Encoder and Decoder**

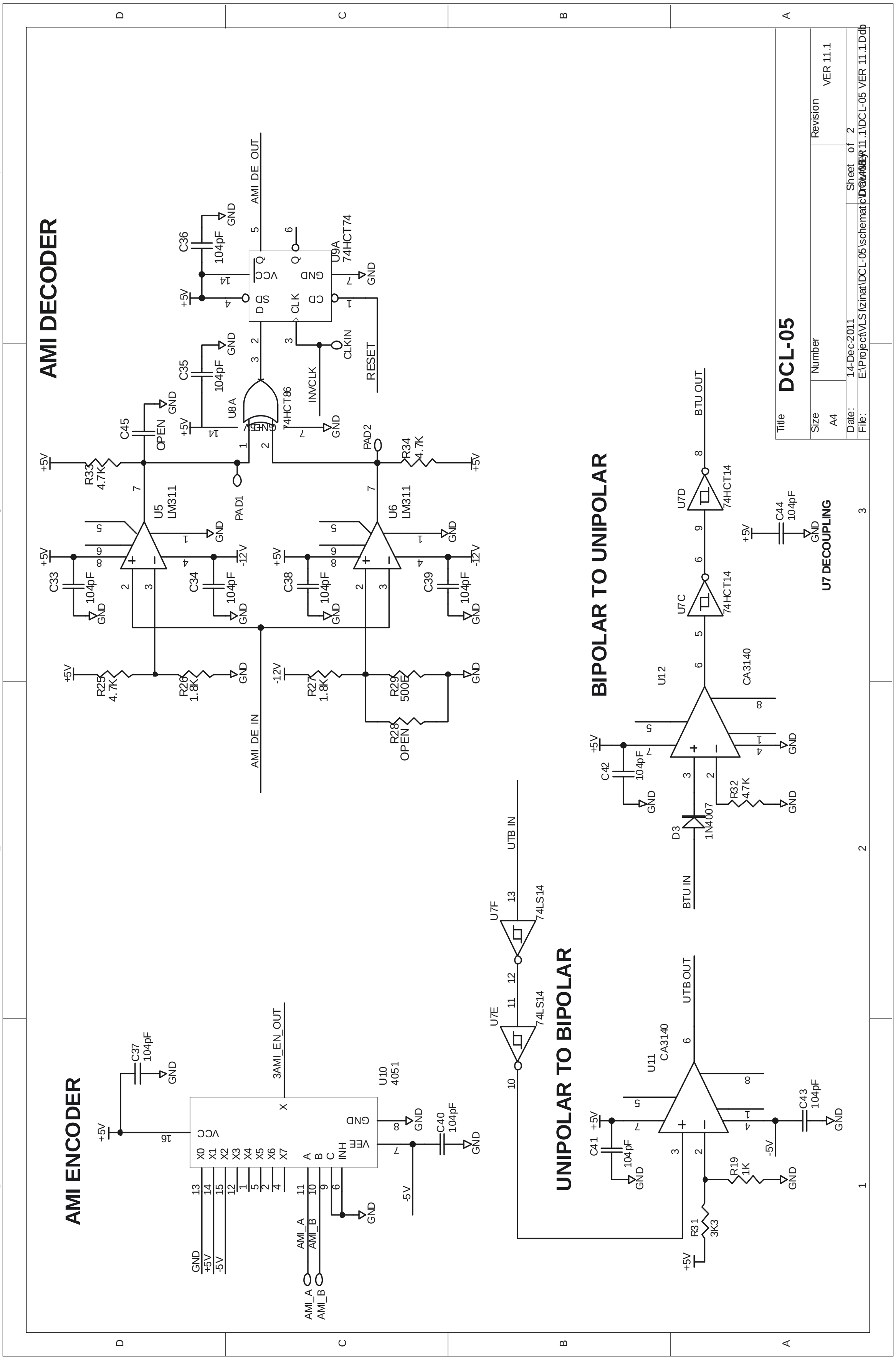
Refer sheet 2 of DCL-05 for the circuit diagram of AMI Encoder and Decoder. The AMI encoded data is obtained from U10 (IC 4051) which is single 8-channel analog MUX/DEMUX, which is used as multiplexer. Three inputs GND, +5V, -5V are fed to its input lines, and AMI_A AND AMI_B are used to control the output of the multiplexer. AMI_A and AMI_B are obtained from the CPLD by programming. AMI Decoder consist of two LM311 (U5 and U6) to separate AMI_A and AMI_B signal from the AMI encoded signal, 74HCT86 (U8) to EXOR recovered AMI_A and AMI_B, and 74HCT74 (U9) to recovered the original data.

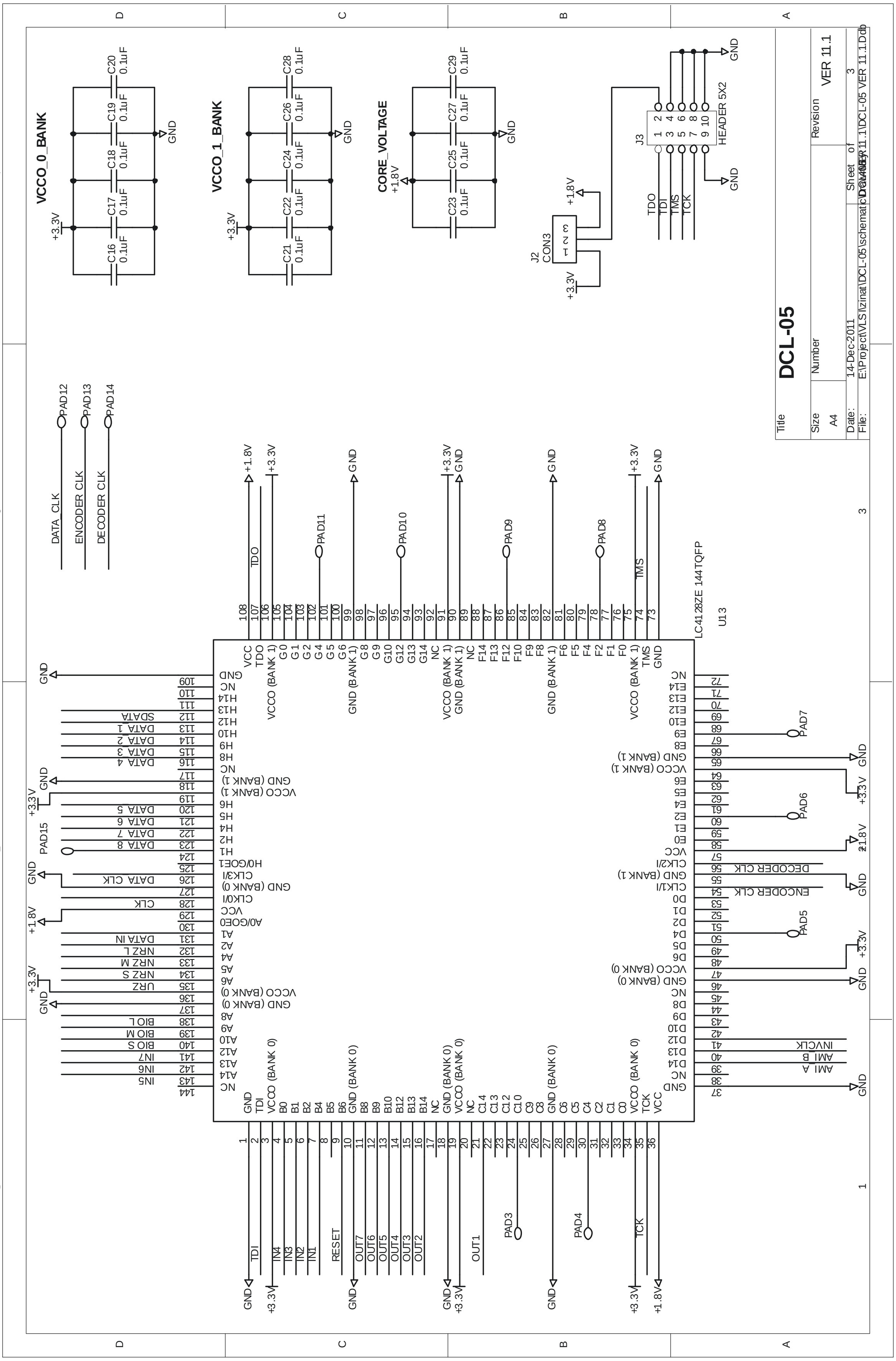
- **Unipolar To Bipolar /Bipolar To Unipolar**

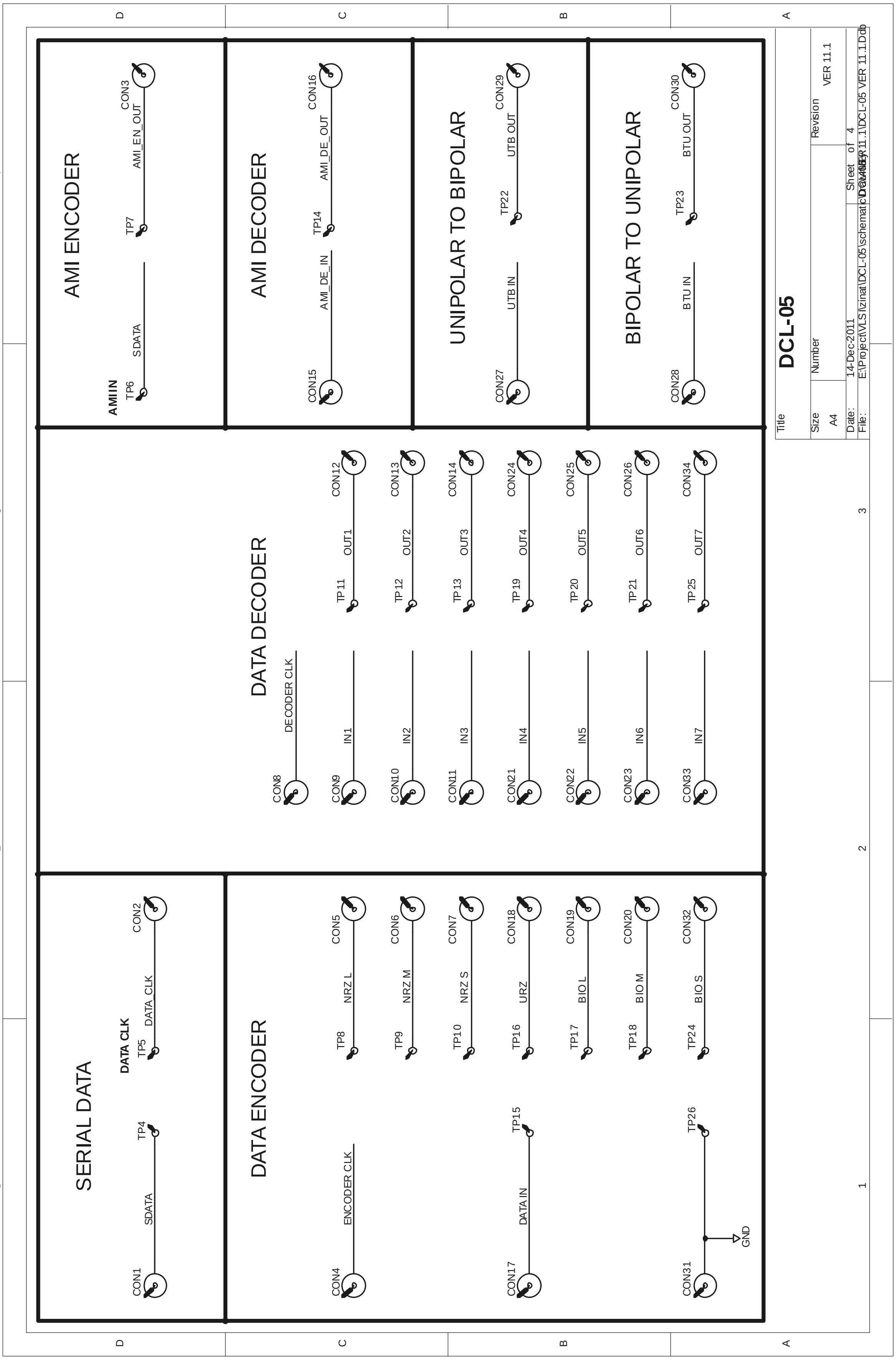
Refer sheet 2 of DCL-05 for the circuit diagram of Unipolar to Bipolar and Bipolar to Unipolar. The UNIPOLAR TO BIPOLAR data is obtained by feeding input data to U20 (IC CA3140) whose output depends upon the Vdd and Vss voltages, which are +5V and –5V respectively. The BIPOLAR TO UNIPOLAR is obtained in the same way by feeding input data to U21 (IC CA3140) whose output depends upon the Vdd and Vss voltages, which are kept at +5V and GND.

CIRCUIT DIAGRAM OF DCL-05




AMI DECODER
AMI ENCODER
BIPOLAR TO UNIPOLAR
UNIPOLAR TO BIPOLAR
U7 DECOUPLING
DCL-05
Title
Size
A4
Number
Revision
VER 11.1
Date:
14-Dec-2011
Sheet of 2
File:
AMI_DE_OUT
AMI_DE_IN
3AMI_EN_OUT
AMI_A
AMI_B
UTB IN
UTB OUT
BTU IN
BTU OUT
CLKIN
INVCLK
RESET
U5 LM311
U6 LM311
U8A 74HCT86
U9A 74HCT74
U10 4051
U11 CA3140
U12 CA3140
U7C 74HCT14
U7D 74HCT14
U7E 74LS14
U7F 74LS14
D3 1N4007
R25 4.7K
R26 1.8K
R27 1.8K
R28 OPEN
R29 500E
R33 4.7K
R34 4.7K
R31 3K3
R19 1K
R32 4.7K
C45 OPEN
PAD1
PAD2


VCCO_0_BANK
VCCO_1_BANK
CORE_VOLTAGE
HEADER 5X2
LC4128ZE 144TQFP
U13
DCL-05
VER 11.1
14-Dec-2011


AMI ENCODER
AMI IN
TP6
SDATA
TP7
AMI_EN_OUT
CON3
AMI DECODER
CON15
AMI_DE_IN
TP14
AMI_DE_OUT
CON16
UNIPOLAR TO BIPOLAR
CON27
UTB IN
TP22
UTB OUT
CON29
BIPOLAR TO UNIPOLAR
CON28
BTU IN
TP23
BTU OUT
CON30
DATA DECODER
CON8
DECODER CLK
CON9 IN1 TP11 OUT1 CON12
CON10 IN2 TP12 OUT2 CON13
CON11 IN3 TP13 OUT3 CON14
CON21 IN4 TP19 OUT4 CON24
CON22 IN5 TP20 OUT5 CON25
CON23 IN6 TP21 OUT6 CON26
CON33 IN7 TP25 OUT7 CON34
SERIAL DATA
CON1
SDATA
TP4
DATA CLK
TP5
DATA_CLK
CON2
DATA ENCODER
CON4
ENCODER CLK
TP8 NRZ L CON5
TP9 NRZ M CON6
TP10 NRZ S CON7
CON17
DATA IN
TP15
TP16 URZ CON18
TP17 BIO L CON19
TP18 BIO M CON20
CON31
GND
TP26
TP24 BIO S CON32
Title
DCL-05
Size
A4
Number
Revision
VER 11.1
Date: 14-Dec-2011
Sheet of 4
File: E:\Project\VLSI\zinat\DCL-05\schematic\DCL-05 VER 11.1\DCL-05 VER 11.1.Ddb
Drawn By:

EXPERIMENT
NO. 1

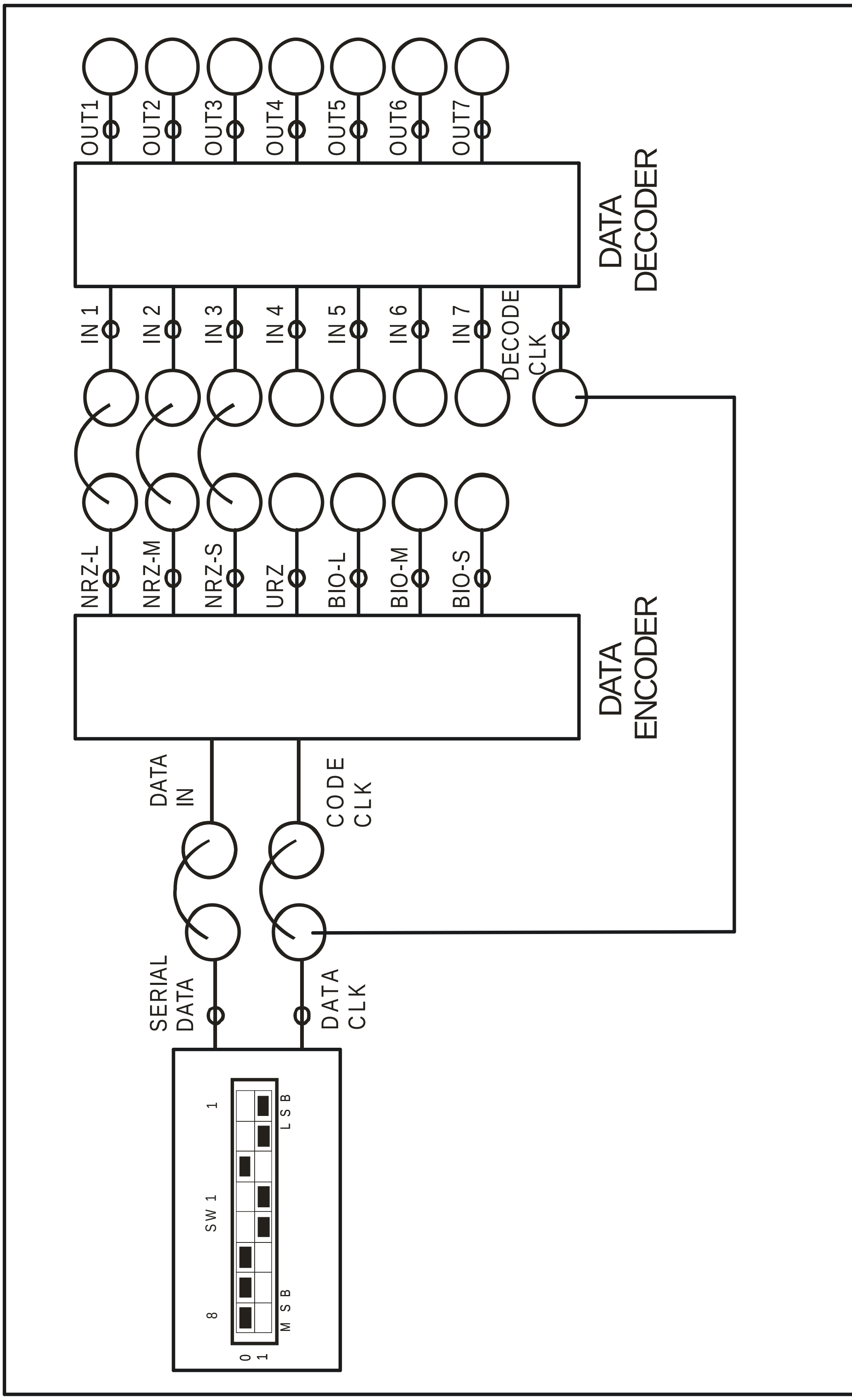


FIG 1.1 BLOCK DIAGRAM FOR CONDITIONING AND RECONDITIONING TECHNIQUES FOR NRZ FORMAT

EXPERIMENT NO. : 1

NAME

Data conditioning and reconditioning techniques for non-return to zero format (NRZ-L, NRZ-M, NRZ-S, UNIPOLAR TO BIPOLAR, BIPOLAR TO UNIPOLAR).

OBJECTIVE

To study of data conditioning and reconditioning techniques for Non-return to Zero Formatsuchas:
(a) Non Return to Zero - Level (NRZ-L)
(b) Non Return to Zero - Mark (NRZ-M)
(c) Non Return to Zero - Space (NRZ-S)
(d) Unipolar to Bipolar-Bipolar to Unipolar.

THEORY

NON - RETURN TO ZERO signal are the easiest formats that can be generated.
These signals do not return to zero with the clock. The frequency component associated with these signals are half that of the clock frequency. The following data formats come under this category. Non-return to zero encoding is commonly used in slow speed communications interfaces for both synchronous and asynchronous transmission. Using NRZ, logic 1 bit is sent as a high value and a logic 0 bit is sent a sa low value.

A) Non-Return to zero - LEVEL - NRZ-L,
B) Non-Return to zero - MARK - NRZ-M
C) Non-Return to zero - SPACE - NRZ-S

A) NON-RETURN TO ZERO - LEVEL (NRZ-L):
This is the most extensively used waveform in digital logics. The data format is very simple where all ‘ones’ are represented by `high’ and all `zeros’ by `low’. The data format is directly available at the output of all digital data generation logics and hence very easy to generate. Here all the transitions take place at the rising edge of the clock.

B) NON-RETURN TO ZERO - MARK (NRZ-M):
These waveforms are extensively used in magnetic tape recording. In this data format, all `ones’ are marked by change in levels and all “zeros’ by no transitions, and the transitions take place at the rising edge of the clock.

C) NON-RETURN TO ZERO - SPACE (NRZ-S),
This type of waveform is marked by change in levels for `zeros’ and no transition for `ones’ and the transitions take place at the rising edge of the clock. This format is also used in magnetic tape recording.

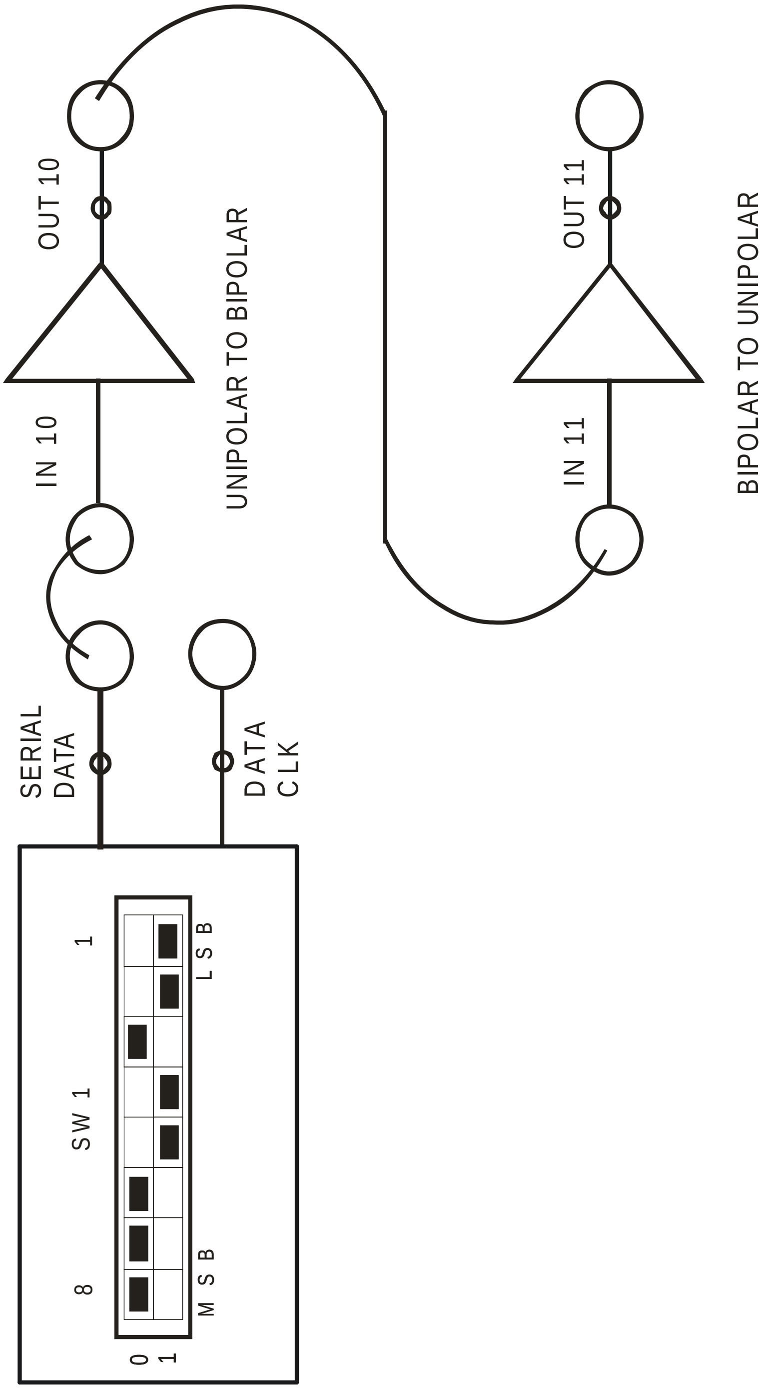


FIG 1.2 BLOCK DIAGRAM FOR UNIPOLAR TO BIPOLAR AND BIPOLAR TO UNIPOLAR TECHNIQUES

D) UNIPOLAR AND BIPOLAR:
Unipolar signals are those signals, which have transition between 0 to +VCC. Bipolar signals are those signals, which have transition between +VCC to -VCC.

EQUIPMENTS

Experimental Kits DCL-05.
Patch Chords.
Power supply.
30MHz Dual Trace Oscilloscope/DSO.

PROCEDURE

1. Refer to the block diagram **Fig. 1.1** and carry out the following connections and switch settings.
2. Connect power supply in proper polarity to the kit**DCL-05** and switch it on.
3. Select desired data pattern using switch **SW1**.
4. Connect **DATA CLK** and **SERIAL DATA** generated on board to **CODE CLK** and **DATA IN** of **DATAENCODER** respectively by means of the patch-chords provided.
5. Observe the encoded signal at respective outputs of **DATAENCODER** on the oscilloscope.
6. For decoding the signal connect **DATA CLK** to **DECODE CLK** and **NRZ-L**, **NRZ-M**, **NRZ-S** output of **DATAENCODER** to respective inputsi.e.**IN1**, **IN2** and **IN3** of **DATADECODER**.
7. Observe the decoded signal at respective outs i.e. **OUT1**, **OUT2** and **OUT3** of **DATADECODER** on the oscilloscope. It should be same as **DATA IN.**
8. Use **RST** switch for clear data observation if necessary.
9. Unipolar to Bipolar / Bipolar to Unipolar (Refer **Fig. 1.2**):
   a. Connect **SERIAL DATA** signal to the input post **IN10**of Unipolar to Bipolar and Observe the Bipolar output at post **OUT10**of Unipolar to Bipolar.
   b. Then connect Bipolar output signal **OUT10** of Unipolar to Bipolar to the input post **IN11**of Bipolar to Unipolar and observe Unipolar output at post **OUT11**of Bipolar to Unipolar. It should be same as **IN10**of Unipolar to Bipolar**.**

OBSERVATION

Observe the following coded signal on the oscilloscope and plot it on the paper.

1. **SERIAL DATA** with respect to **DATA CLK**. **FIG. 1.3(a)**
2. Coded data **NRZ-L** with respect to **DATA IN**. **FIG. 1.3(b)**
3. Coded data **NRZ-M** with respect to **DATA IN**. **FIG. 1.3(c)**
4. Coded data **NRZ-S** with respect to **DATA IN**. **FIG. 1.3(d)**
5. **OUT1**with respect to **DATA IN**. **FIG. 1.3(e)**
6. **OUT2** with respect to **DATA IN**. **FIG. 1.3(f)**
7. **OUT3** with respect to **DATA IN**. **FIG. 1.3(g)**
8. Bipolar output at **OUT10**with respect to **IN10**. **FIG. 1.3(h)**
9. Unipolar output at **OUT11**with respect to**IN10**. **FIG. 1.3(i)**

CAPTURED WAVEFORM

CH 1: DATA CLK (266 KHz) & CH 2: SERIAL DATA (00011011)

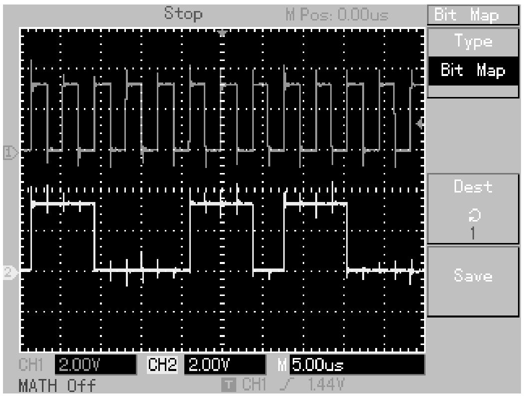


FIG. 1.3(a)

CH 1:DATA IN& CH 2:NRZ-L

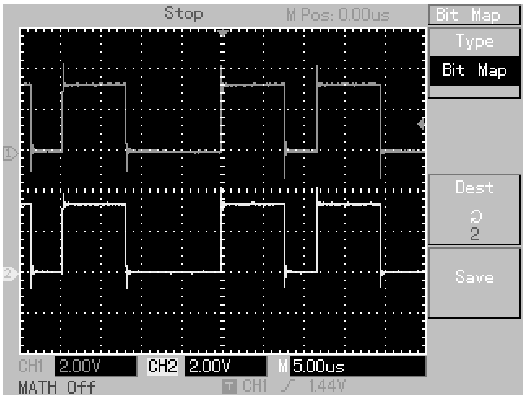


FIG. 1.3(b)

CH 1: DATA IN& CH 2: NRZ-M

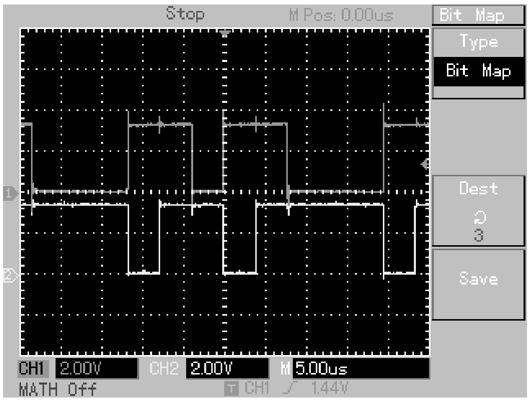


FIG. 1.3(c)

CH 1: DATA IN& CH 2: NRZ-S

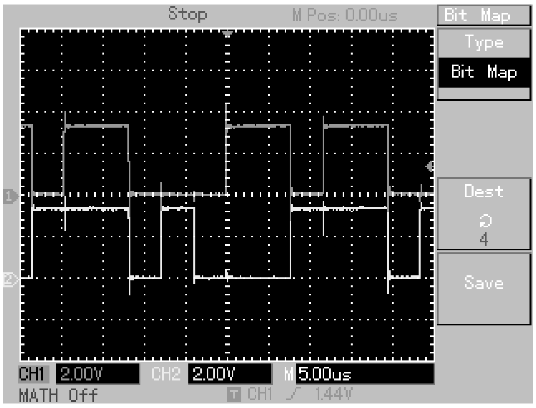


FIG. 1.3(d)

CH 1:DATA IN& CH 2: OUT1

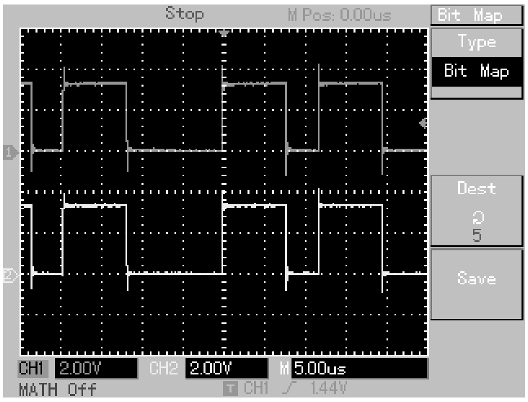


FIG. 1.3(e)

CH 1: DATA IN& CH 2: OUT2

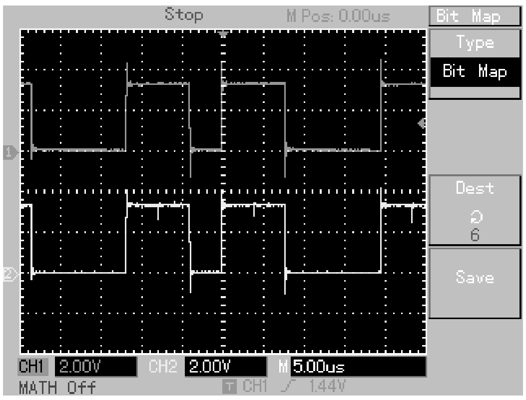


FIG. 1.3(f)

CH 1: DATA IN& CH 2: OUT3

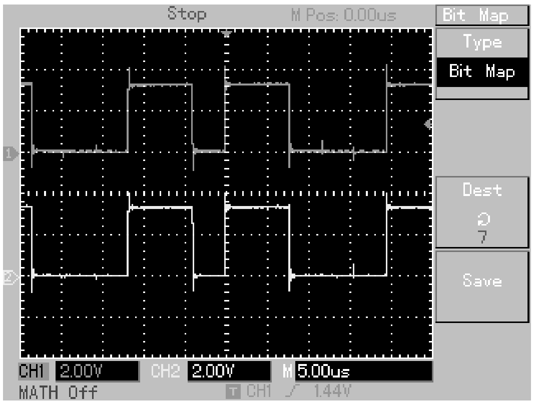


FIG. 1.3(g)

CH 1: IN10& CH 2:OUT10

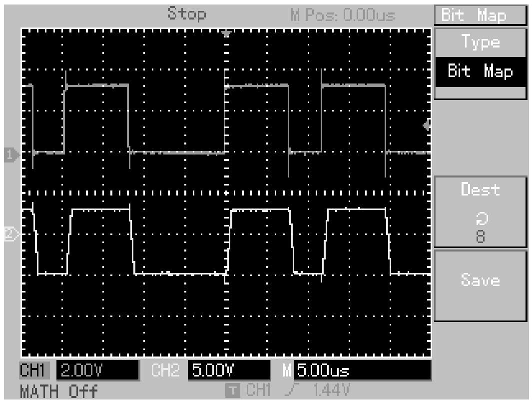


FIG. 1.3(h)

CH 1: IN10& CH 2: OUT11

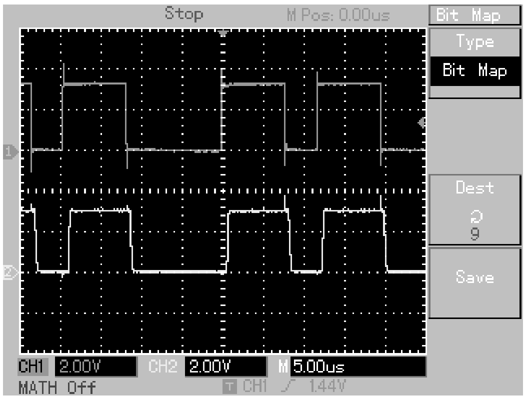


FIG. 1.3(i)

CONCLUSION:

The NRZ-L, NRZ-M, NRZ-S coded signals have a frequency component, that is equal to half the frequency of the coding (reference) clock. The recovered data is observed to have a very small phase lag with respect to the transmitted data.

EXPERIMENT
NO. 2

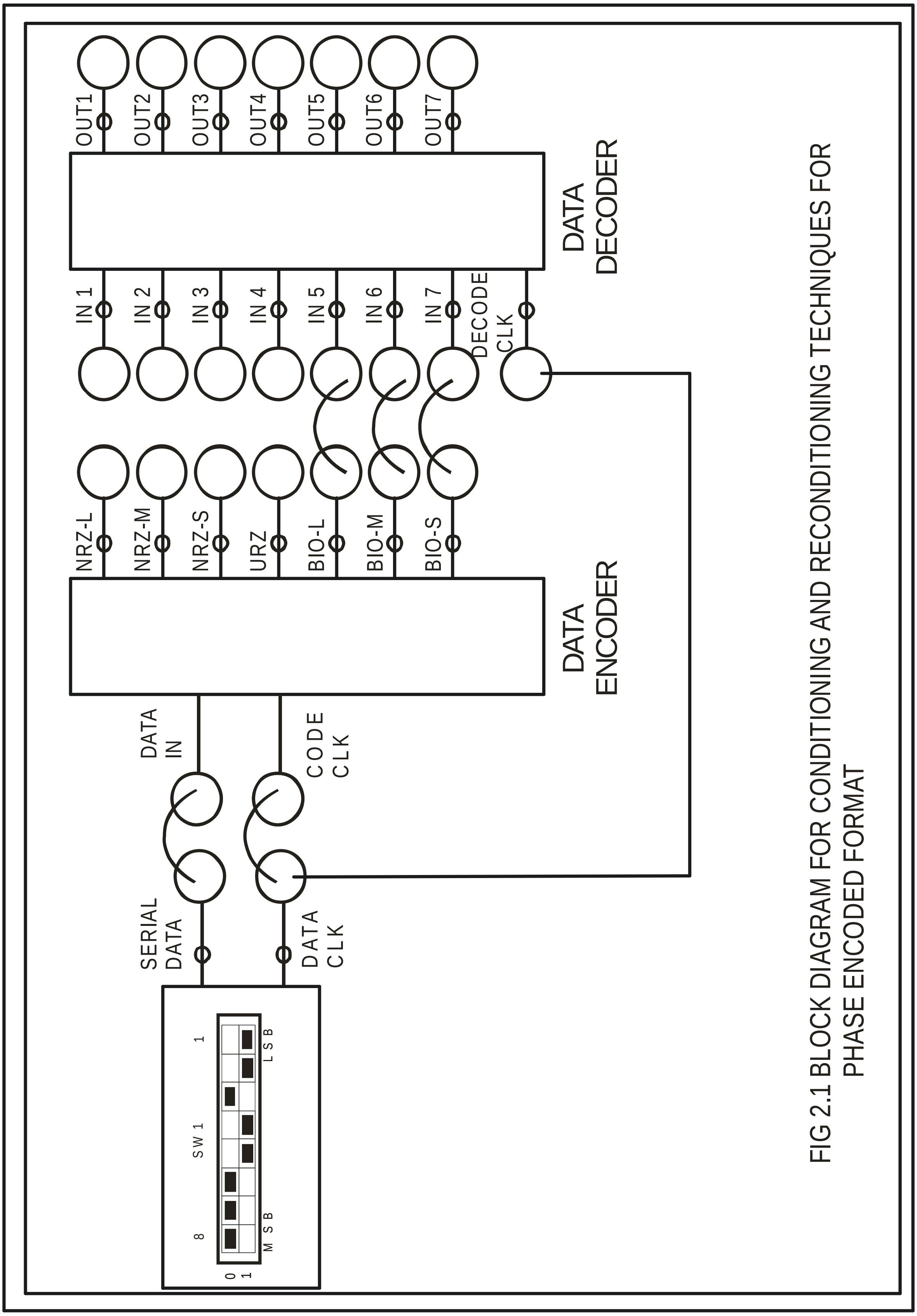


FIG 2.1 BLOCK DIAGRAM FOR CONDITIONING AND RECONDITIONING TECHNIQUES FOR PHASE ENCODED FORMAT

EXPERIMENT NO. : 2

NAME

Data conditioning and reconditioning techniques for phase encoded format (BIO-L, BIO-M, BIO-S).

OBJECTIVE

To study data conditioning and reconditioning techniques for Phase Encoded Format (Biphase Signals) such as:
(a) Biphase -Level (Manchester Coding)
(b) Biphase - Mark
(c) Biphase- Space

THEORY

This phase -encoded -group consists of:
a) Biphase - Level (Popularly known as Manchester Coding)
b) Biphase - Mark,
c) Biphase - Space.

These schemes are used in magnetic recording, optical communications and in satellite links. These phase encoded signals are special in the sense that they are composed of both the in phase and out of phase components of the clock:

A) BIPHASE-LINE CODING (BIPHASE-L) - (MANCHESTER CODING)
With the Biphase-L `one’ is represented by a half bit wide pulse positioned during the first half of the bit interval and a `zero’ is represented by a half bit wide pulse positioned during the second half of the bit interval.

B) BIPHASE MARK CODING (BIPHASE-M)
With the Biphase-M, a transition occurs at the beginning of every bit interval. A `one’ is represented by a second transition, half bit later, whereas a zero has no second transition.

C) BIPHASE SPACE CODING (BIPHASE -S):
With a Biphase-S, a transition occurs at the beginning of every bit interval. A `zero’ is marked by a second transition, one half bit later; `one’ has no second transition.

The coding of basic data NRZ-L into Biphase-L, Biphase-M, and Biphase-S format can be understand easily by referring to circuit diagram and Waveforms.

Biphase-Line Coding is a synchronous clock coding technique used by the OSI physical layer (in LAN) to encode the clock and data of a synchronous bit stream. In this technique, the actual binary data to be transmitted over the cable are not sent asa sequence of logic 1's and 0's (known technically as Non Return to Zero (NRZ)). Instead, the bits are translated into a slightly different format that has a number of advantages over using straight binary encoding (i.e. NRZ).

Biphase-Line Coding follows the rules shown below:

Original	Data Value Sent
Logic 0	0 to 1 (upward transition at bit centre)
Logic 1	1 to 0 (downward transition at bit centre)

Example of Biphase-Line Coding

The pattern of bits " 0 1 1 1 1 0 0 1 " encodes to " 01 10 10 10 10 01 01 10".

The recovery circuit of Biphase coded signal is quiet simple as compared to NRZ or URZ signals because the bi-phase signals have one transition per cycle of the clock irrespective of the transmitted data. So these signals ensure sufficient number of transitions in the data stream. But one disadvantage in bi-phase signals is that they do not provide phase continuity in the transmitted data stream.

EQUIPMENTS

Experimental Kits DCL-05.
Patch Chords.
Power supply.
30MHz Dual Trace Oscilloscope/ DSO.

PROCEDURE

1. Refer to the block diagram **Fig. 2.1** and carry out the following connections and switch settings.
2. Connect power supply in proper polarity to the kit **DCL-05** and switch it on.
3. Select desired data pattern using switch **SW1**.
4. Connect **DATA CLK** and **SERIAL DATA** generated on boardto **CODE CLK** and **DATA IN** post of **DATA ENCODER** respectively by means of the patch-chords provided.
5. Observe the encoded signal at respective outs i.e. **BIO-L**, **BIO-M**, **BIO- S** of **DATAENCODER** on the oscilloscope.
6. For decoding the signal connect **DATA CLK** to **DECODE CLK** and **BIO-L, BIO-M, BIO-S** to **IN5, IN6, IN7**of **DATA DECODER**respectively.
7. Observe the decoded signal at **OUT5**, **OUT6** and **OUT7**post of **DATADECODER OUT** on the oscilloscope. It should be same as **DATA IN.**
8. Use **RST** switch for clear data observation if necessary.

OBSERVATION

Observe the following coded signal on the oscilloscope and plot it on the paper.

1. **SERIAL DATA** with respect to **DATA CLK**. **FIG. 2.2(a)**
2. Coded data **BIO-L** with respect to **DATA IN**. **FIG. 2.2(b)**
3. Coded data **BIO-M** with respect to **DATA IN**. **FIG. 2.2(c)**
4. Coded data **BIO-S** with respect to **DATA IN**. **FIG. 2.2(d)**
5. Decoded data **BIO-L** with respect to **DATA IN**. **FIG. 2.2(e)**
6. Decoded data **BIO-M** with respect to **DATA IN**. **FIG. 2.2(f)**
7. Decoded data **BIO-S** with respect to **DATA IN**. **FIG. 2.2(g)**

CAPTURED WAVEFORM

CH 1: DATA CLK (266 KHz) & CH 2: SERIAL DATA (00011011)

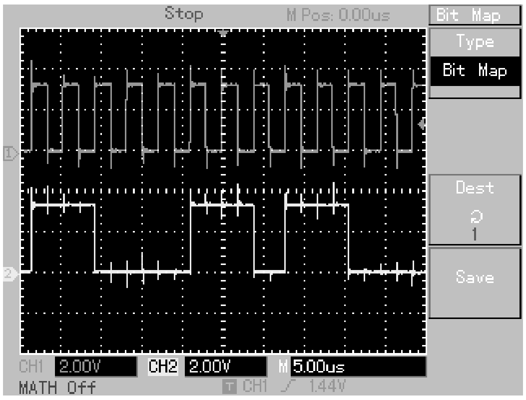


FIG. 2.2 (a)

CH 1: DATA IN& CH 2: BIO-L

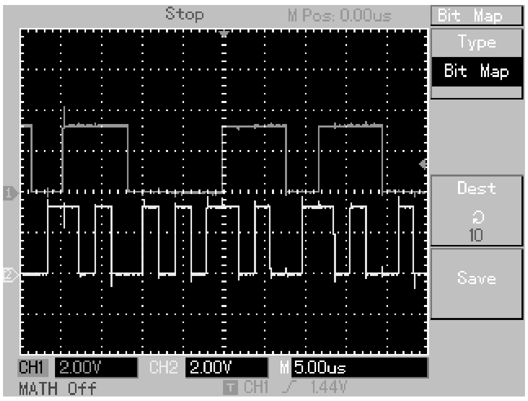


FIG. 2.2 (b)

CH 1: DATA IN & CH 2: BIO-M

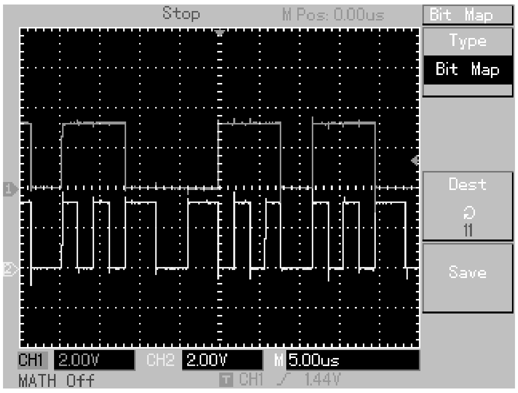


FIG. 2.2 (c)

CH 1: DATA IN& CH 2: BIO-S

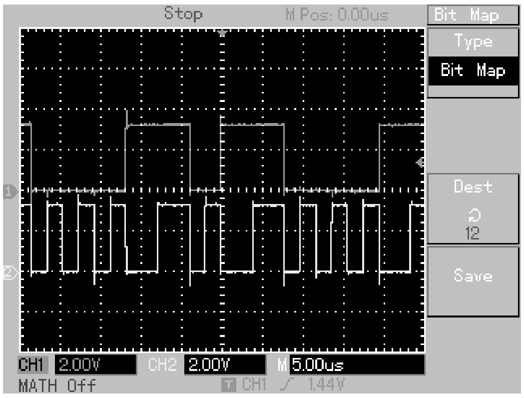


FIG. 2.2 (d)

CH 1: DATA IN& CH 2: OUT5

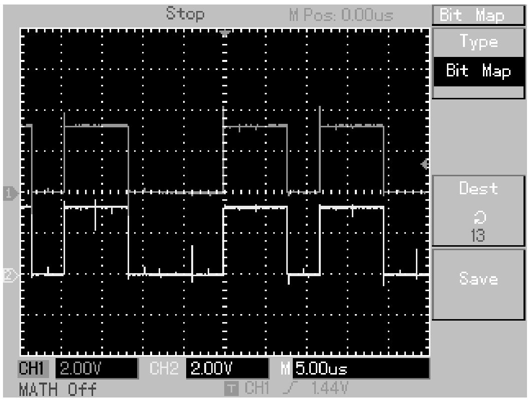


FIG. 2.2 (e)

CH 1: DATA IN& CH 2: OUT6

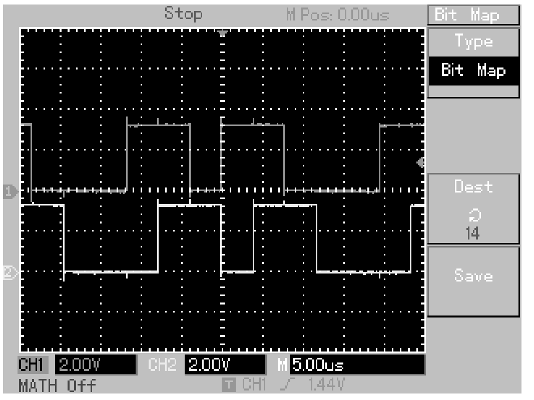


FIG. 2.2 (f)

CH 1: DATA IN& CH 2: OUT7

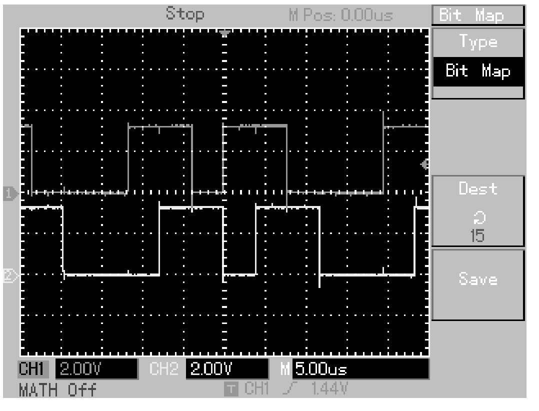


FIG. 2.2 (g)

CONCLUSION:

The Biphase-L, Biphase-M, Biphase-S coded signals have frequency component equal to that of the data clock and these signal are composed of both the in phase and out of phase components of the data clock. The recovered data has a very small phase lag with respect to the transmitted data.

EXPERIMENT
NO. 3

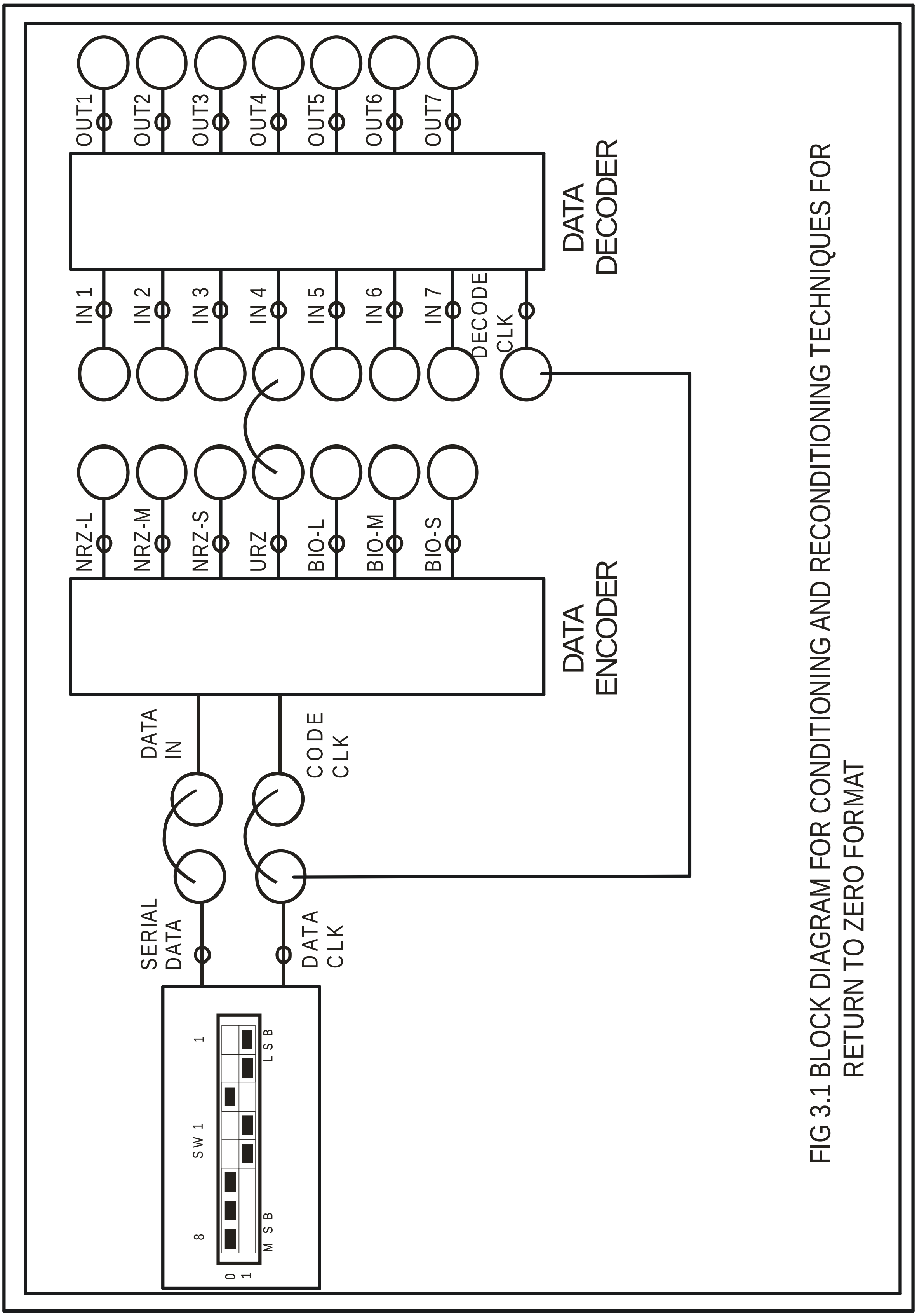


FIG 3.1 BLOCK DIAGRAM FOR CONDITIONING AND RECONDITIONING TECHNIQUES FOR RETURN TO ZERO FORMAT

EXPERIMENT NO.: 3

NAME

Data conditioning and reconditioning techniques for return to zero formatand multilevel binary format (URZ, RZ-AMI).

OBJECTIVE

To study data conditioning and reconditioning techniques for Return to Zero format and Multilevel binary format. such as:
(a) Unipolar Return to Zero Coding (URZ)
(b) Return to Zero - Alternate Mark Inversion Coding (RZ-AMI).

THEORY

A) RETURN TO ZERO SIGNALS:
These signals are called “Return to Zero signals”, since they return to `zero’ with theclock. In this category, only one data format, i.e., the unipolar return to zero (URZ):With the URZ a `one’ is represented by a half bit wide pulse and a `zero’ is
represented by the absence of a pulse.

B) MULTILEVEL SIGNALS:
Multilevel signals use three or more levels of voltages to represent the binary digits, `one’ and `zero’ - instead of the normal `highs’ and `lows’
Return to zero - Alternative Mark Inversion (RZ - AMI) is the most commonly used multilevel signal This coding scheme is most often used in telemetry systems. In this scheme, `one’ are represented by equal amplitude of alternating pulses, which alternate between a +5V and -5V. These alternating pulses return to 0 volt, after every half bit interval. The `zeros’ are marked by absence of pulses.

The coding of basic data NRZ-L into URZ and RZ-AMI format can be understand easily by referring to circuit diagram and Waveforms.

For decoding the URZ coded data, first of all the clock is recovered from the incoming coded data by using phase locked loop techniques. Since the URZ signal has a frequency component equal to the clock, the bi-directional monoshot and OR gate should be eliminated in this application.

For recovery of clock from RZ-AMI, first the RZ-AMI should be converted to URZ by standard techniques. Then the clock is recovered.

Refer the circuit diagram and waveforms for the decoding techniques.

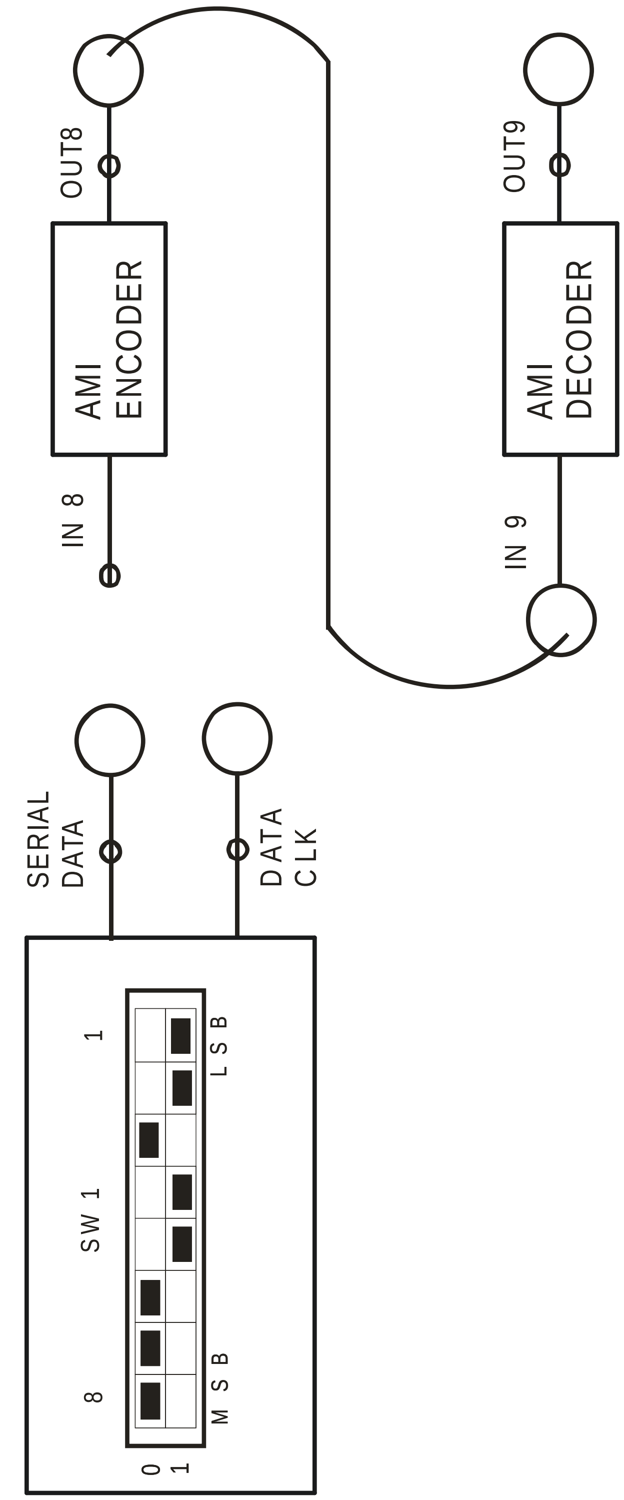


FIG 3.2 BLOCK DIAGRAM FOR CONDITIONING AND RECONDITIONING TECHNIQUES FOR MULTILEVEL BINARY FORMAT

EQUIPMENTS

Experimental Kit DCL-05.
Patch Chords.
Power supply.
30MHz Dual Trace Oscilloscope/ DSO.

PROCEDURE

1. Refer to the **Fig. 3.1** and carry out the following connections and switch settings.
2. Connect power supply in proper polarity to the kit **DCL-05** and switch it on.
3. Select desired data pattern using switch **SW1**.
4. Connect **DATA CLK** and **SERIAL DATA** generated on board to **CODE CLK** and **DATA IN** post of **DATA ENCODER** respectively by means of the patch-chords provided.
5. Observe the encoded signal at **URZ** post of **DATAENCODER** on the oscilloscope.
6. For decoding the signal connect **DATA CLK** to **DECODE CLK** and **URZ** of **DATAENCODER** to **IN4** of **DATADECODER**.
7. Observe the decoded signal at **OUT4** of **DATADECODER** on the oscilloscope. It should be same as **DATA IN.**
8. Use **RST** switch for clear data observation if necessary.
9. AMI Encoding / Decoding (Refer **Fig. 3.2**).
    a. Observe the signal at the input post **IN8**of **AMI ENCODER**. It should be same as **SERIAL DATA**. And observe the **AMI ENCODER** output at post **OUT8**of**AMI ENCODER**.
    b. Then connect **OUT8**of**AMI ENCODER** to the input post **IN9**of **AMI DECODER** and observe output at post **OUT9**of **AMI DECODER**. It should be same as **IN8**of **AMI ENCODER.**

OBSERVATION

Observe the following coded signal on the oscilloscope and plot it on the paper.
1. **SERIAL DATA** with respect to **DATA CLK**. **FIG. 3.3(a)**
2. Coded data **URZ** with respect to **DATA IN**. **FIG. 3.3(b)**
3. Decoded data at **OUT4**of **DATADECODER** with respect to **DATA IN**. **FIG. 3.3(c)**
4. **OUT8**of **AMI ENCODER** with respect to **IN8**of **AMI ENCODER**. **FIG. 3.3(d)**
5. **OUT9**of **AMI DECODER** with respect to **IN8**of **AMI ENCODER**. **FIG. 3.3(e)**

CAPTURED WAVEFORM

CH 1: DATA CLK (266 KHz) & CH 2: SERIAL DATA (00011011)

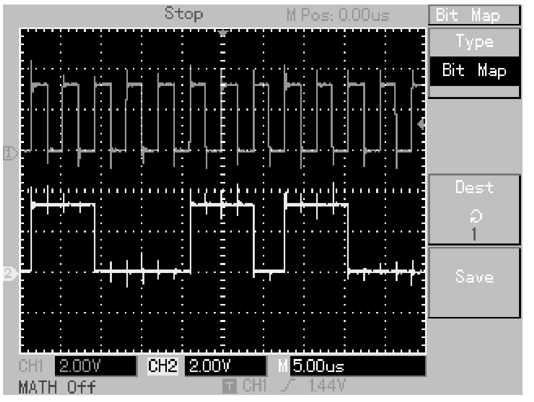


FIG. 3.3(a)

CH 1: DATA IN& CH 2: URZ

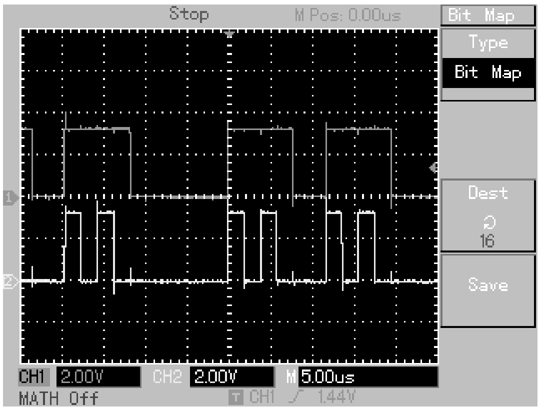


FIG. 3.3(b)

CH 1: DATA IN& CH 2: OUT4

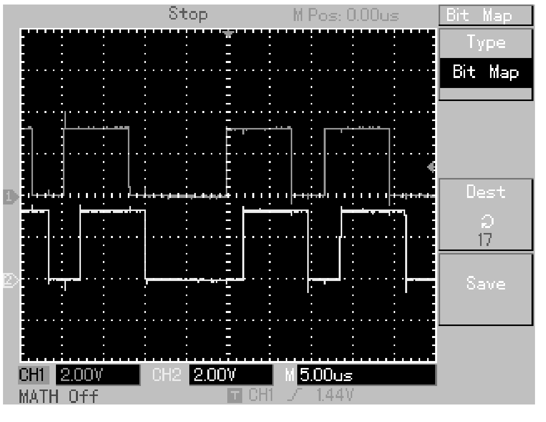


FIG. 3.3(c)

CH 1: IN8 & CH 2: OUT8

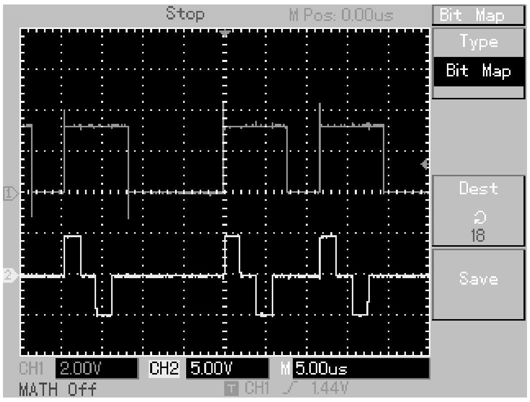


FIG. 3.3(d)

CH 1: IN8 & CH 2: OUT9

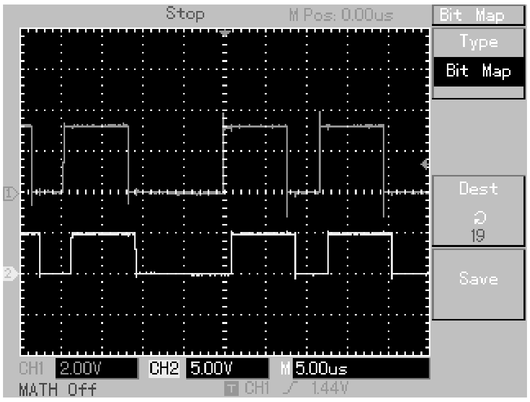


FIG. 3.3(e)

<u>CONCLUSION</u>:

The URZ coded signal and RZ-AMI Coded signal have frequency component equal to that of the data clock and the signals are in phase with the clock. The recovered data is observed to have a very small phase lag with respect to the transmitted data.