AKADEMIKA

DCL-01
ANALOG SIGNAL SAMPLING AND RECONSTRUCTION KIT

EXPERIMENTAL MANUAL

…. A MESSAGE FROM

AKADEMIKA

Today's system designers are faced with tomorrow's problems. DIGITAL COMMUNICATION is one of the important subject need to teach while learning electronics.
It is our vision to provide you with the product you need for training ensuring lasting reliability & quality**.**

OUR MOTTO;

- Light years ahead – refers to leadership.

As leaders in our industry in India, we are totally committed to servicing as the standard against which all are measured in the areas of

• Design • Quality • Value • Delivery • Support.

We are truly light years ahead of our competition in this area. That means that you our valued customers are guaranteed satisfaction.

As you will move through this manual you will quickly discover that we have complete, truly innovative & superior training products. We are so committed to quality that we back our products with a complete comprehensive warranty.

AKADEMIKA LAB SOLUTIONS

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SAFETY RULES

Carefully follow the instructions contained in this manual as they provide you with important points on safety during the installation, use and maintenance. Keep this manual always with you for easy reference.

Arrange all accessories in order after unpacking, so that their integrity is checked with respect to the packing list. Also ensure that no visible damage as such appear on any accessories.

Before connecting the power supply to the kit, be sure that the jumpers and connecting chords are connected correctly as per experiment.

In DCL-01 kit, signals are to be monitored with an oscilloscope, or with the help of indicators as explained in the manual. For observation of signals on oscilloscope either use X10 (Attenuation Probe) or 180Ω resistance in series with normal oscilloscope probe.

This kit must be employed only for the use for which it has been conceived, i.e. as educational kit and must be used under the direct survey of expert personnel. Any other use is improper and so dangerous. The manufacturer cannot be considered responsible for eventual damages due to improper, wrong or unreasonable uses.

In case of any fault or malfunctioning in the trainer kit, turn off the power supply and do not tamper the kit. In case servicing is required, contact the service center for technical assistance.

The kits are liable to malfunction/under-perform if they are not operated under standard environmental conditions of temperature and humidity.

WARRANTY

This kit is warranted against defects in workmanship and materials. Any failure due to defect in either workmanship or material should occur under normal use within a year from the original date of purchase, such failure will be corrected free of charge to the purchaser by repair or replacement of defective part or parts. When the failure is result of user's neglect, natural disaster or accident, we charge for repairs regardless of the warranty period. The warranty does not cover perishable items like connecting chords, Crystals, etc. and other imported items.

This warranty is subject to the following conditions and limitations. The warranty is void and inapplicable if the defective product is not brought or sent to our authorized service center or sales outlet within the warranty period. Defective product is, on Akademika Lab Solutions sole judgment. The defective product will be replaced with new one or repaired without charge or with charge.

In the warranty period if the service is needed, purchaser should get in touch with the service center or sales outlet. The purchaser should return the product to the service center or sales outlet at his or her sole expense. The loss and damage in transit will be outside the preview of this warranty. A returned product must be accompanied by a written description of the defects. Type and Model No. of kit has to be mentioned specifically. We return the product to the purchaser at our expense. In case that warranty does not cover the product on Akademika Lab Solutions judgment, we repair the product after obtaining prior permission from purchaser who receives an estimate statement about repairing charges. In such case, Akademika Lab Solutions bares the transporting expenses required to send back all the repaired products for the moment, and then repairs and transporting expenses will be charged against the purchaser by the statement of accounts.

When the authorized sales agents sell our products, they must notify the purchaser of the warranty contents, but have no rights to stretch the meaning of original warranty contents or offer additional warranty. Akademika Lab Solutions does not provide any other promise or suggestive warranty and hold no liability for the damage caused by negligence, abnormal use or natural disaster. Akademika Lab Solutions is not responsible for the damages even if it is notified of above dangers in advance as well.

For more special service or overall repairs, maintenance and up-gradation of products, be sure to contact our service center or sales outlet.

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TECHNICAL SPECIFICATIONS

Signal
Internal frequency: 1 KHz, 2 KHz.
Amplitude: (0 - 5V)
External frequency: Up to 3 KHz.
Amplitude: (0 - 5V)

Sampling
Internal frequency: 2 KHz, 4 KHz, 8 KHz, 16 KHz, 32 KHz, and 64 KHz.
Duty cycle: 10% - 90% selectable in steps of 10%.
External frequency: Up to 64 KHz.
Duty cycle: 10% - 90%
Amplitude: (0 - 5V)
Natural sampling circuit
Sample and Hold circuit
Flat Top sampling circuit

Reconstruction
2^{nd} order and 4^{th} order low pass butter-worth filters.

Switch Faults
4 Switch Faults are provided on board to study different effects on circuit.

Interconnections
2mm sockets and connecting chords are provided for connection on board.

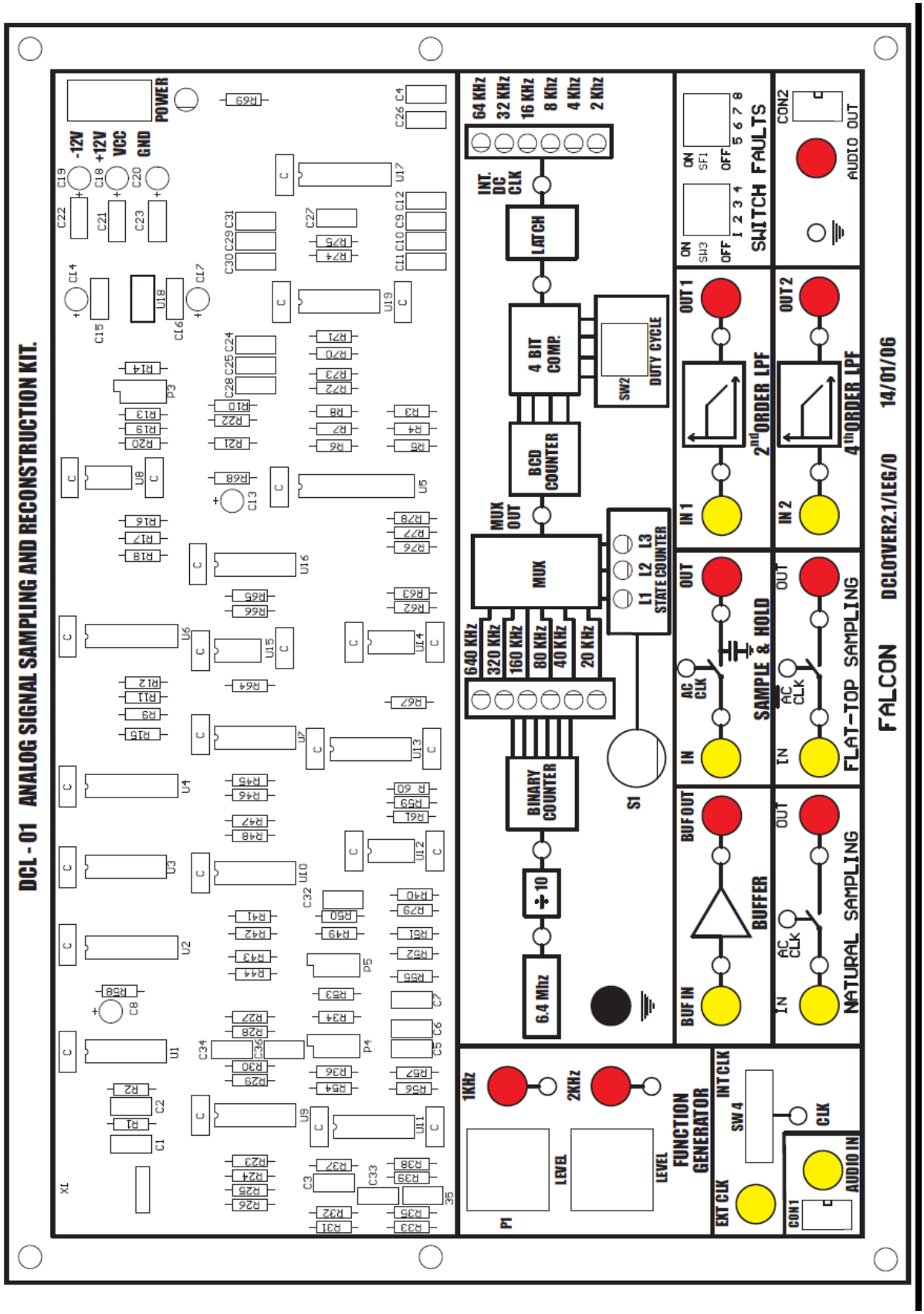
Test Points
All relevant test points are provided onboard to observe intermediate signals.

Supply
-12V, +12V, +5V, GND

Accessories

	DCL -01		Quantity
1	Mini Links PCS2 Patch cord	Male To Male	6
2	Short Links PCS2 Patch cord	Male To Male	2
3	DCL-01 EXPT Manual		1
4	Power Supply		1
5	Power cord		1

FUNCTIONAL BLOCK



INTRODUCTION

AKADEMIKA with the set of trainer kits introduces the user to Principles of Digital Communications.
Digital Communication Systems convey information by using only a finite set of discrete symbols.
"DCL-01: ANALOG SIGNAL SAMPLING AND RECONSTRUCTION KIT" is an introductory trainer kit to enable students to understand the principles of ANALOG SIGNAL SAMPLING AND RECONSTRUCTION.
The single-board "DCL-01" is easy to carry around in the Laboratory and perform experiments. This unit provides the user sine wave of two different frequencies (1 KHz and 2 KHz), whose amplitude can be varied from 0V to 5V by using the pots P1 and P2 respectively. It also provides the user provision to select a sampling frequency from among the 6 different sampling frequencies available along with discrete variation in pulse widths from 10% to 90% of the duty cycle in steps of 10%. The unit has provision to accept external signal frequency and sampling pulse input. All onboard signals can be easily inter-connected using Connecting cords. All onboard signals are Phase-Locked, to enable the learner to observe a stationary signal on an oscilloscope. Test points are brought out on board and identified. The trainer has a complete circuit-mimic inscribed on the PCB.

Principles of Analog Signal Sampling and Reconstruction

Analog source of information produces an output that gives continuous possible values at any given time. Analog signal is an electrical waveform.
The sound pressure from an Orchestra is an analog source and the voltage from a microphone responding to the sound waves represents an analog signal.
Digital source is one with an output that can have only one of the finite sets of discrete values at any time. Temperature is an analog quantity, but when combined with an ON/OFF thermostat, combination can be digital source. Digital signal is defined as an electrical waveform having one of a finite set of possible amplitudes at any time.
Analog and Digital information signals defined are assumed to be `base-band' unless otherwise specified. A base band waveform is one having its largest spectral components clustered in a band of frequencies near zero frequency. The term `low' is often used to mean the same as `base-band' All practical low pass messages will have a frequency above which their spectral components may be considered negligible. We shall call this frequency for a message labeled f(o), the spectral extent of the message (unit is radians/sec).

Sampling Principles

When an analog message is conveyed over an Analog Communication System, the full message is typically used at all times. To send the same analog signal over a Digital Communication System, only its samples are required to be transmitted at periodic intervals. The receiver will receive only samples of the message. It must attempt to re-construct the original message at all times from its samples only.
Anyone associated with Digital Communication System has to know the Principles of Sampling and Re-Construction. It may seem astonishing that samples of a message and not the entire waveform, which can adequately describe all the information in a signal. However, we shall find that under some reasonable conditions, a message can be recovered exactly from its samples, even at times in between samples.

Sampling Theorem For Low Pass Random Signals

Let m (t) is a signal, which is band-limited such that its highest frequency spectral component is fm. Let the values of m (t) be determined at regular intervals separated by times Ts < 1/2fm, i.e., the signal is periodically sampled every Ts second. Then these samples m (n Ts) where n is an integer, uniquely determine the signal and the signal may be re-constructed from these samples with no distortion. Ts are the sampling time.

CIRCUIT DESCRIPTION

- **Sine Wave Generation**

This section basically provides synchronized sine wave of 1 KHz and 2KHz. The 6.4 MHz Crystal Oscillator generates a 6.4 MHz clock. It is divided by 2 decade counter and 2 ripple counter to get the 16 KHz frequency. This signal is fed to serial to parallel shift register, which generates stare case sine wave output, by serial shift operation. The serial shift register U9 (IC 74LS164) has a resistive ladder network at the output. For 16 shifts of the register, one stare case sine wave is produced. So if a 16 KHz clock is fed to the shift register, 1 KHz sine wave is generated. The active filter at the output suppresses the ripple and also takes care of the impedance matching. After filtering we get smooth sine wave output. Similarly by using 32 KHz frequency generated from same crystal, sine wave of 2 KHz is generated by serial shift operation.

- **Sampling Frequency**

The 6.4 MHz Crystal oscillator generates the 6.4 MHz clock. The decade counter U2A (IC 74HC390) divides the frequency by 10 and the ripple counter U3A (IC 74HCT393) generates the basic sampling frequencies 640 KHz to 20 KHz and the other control frequencies.

The basic sampling frequency is given to a U5 (GAL16V8), which acts as multiplexer. For each “Press” on the frequency select switch, the output of the state counter increases by one and it counts from 000 to 101. As the state counter counts from 000 to 101, the corresponding input of the mux is switched to the output. As soon as the count reaches 110, the output of the 3 to 8 decoder resets the state counter and the whole cycle repeats. Also LED connected to the output of the decoder is switched ON, which indicates the sampling frequency selected. Refer the truth table for better understanding.

TRUTH TABLE

0 – LED OFF
1 – LED ON

L1 L2 L3	FREQUENCY
0 0 0	640KHz
0 0 1	320KHz
0 1 0	160KHz
0 1 1	80KHz
1 0 0	40KHz
1 0 1	20KHz

Selected frequency is fed to Duty Cycle control circuit.

- **Duty Cycle**

Refer to the circuit diagram as shown later in this manual sheet 1 of 5 of **DCL-01**. The BCD counter U4 (74HC390) counts from 0000 to 1001. This is connected to the A inputs of the comparator U6 (IC 74LS85). The 4 way DIP switch can be configured such that the B inputs of the comparator varies from 0001 to 1001 and the frequency of the A<B output of the comparator is 10 times less than the frequency of the square wave, that is fed to the input of the BCD counter. Now the duty cycle of the A<B output of the comparator varies from 10% to 90% as the settings of the 4 way DIP switch varies from 0001 to 1001. Now available clock frequencies are divided by 10. Thus we get sampling frequency from 64 KHz to 2 KHz.
Switch is provided to select internally generated clock or External clock or square wave (TTL).

- **Sampling Section**

Refer to the circuit diagram as shown later in this manual sheet 3 of 5 of **DCL-01**. The unit has three sections namely, Natural Sampling Circuit, Sample and Hold Circuit and Flat Top sampling circuit. The sine wave generated is fed as input to the sampling switch U13 (IC CD4066). This samples the analog input at the rate equal to the sampling frequency signal. For sample and hold circuit, The Sine wave is fed to the U13B (IC 4066) which samples the signal and the output is taken across a capacitor, which holds the sample until next sample arrives. Similarly for the Flat Top sampling the sine wave is fed to the U13C (IC 4066) In this the sampling takes place at first switch same as that of the S/H circuit and then at the second switch U13D (IC 4066) which again samples the output, but now the sampling clock fed for sampling is the inverted clock. Output of this section is hold portion from S/H section output. This gives the Flat Top sampled output, which is then passed through the buffer for better output.

- **Filter Section**

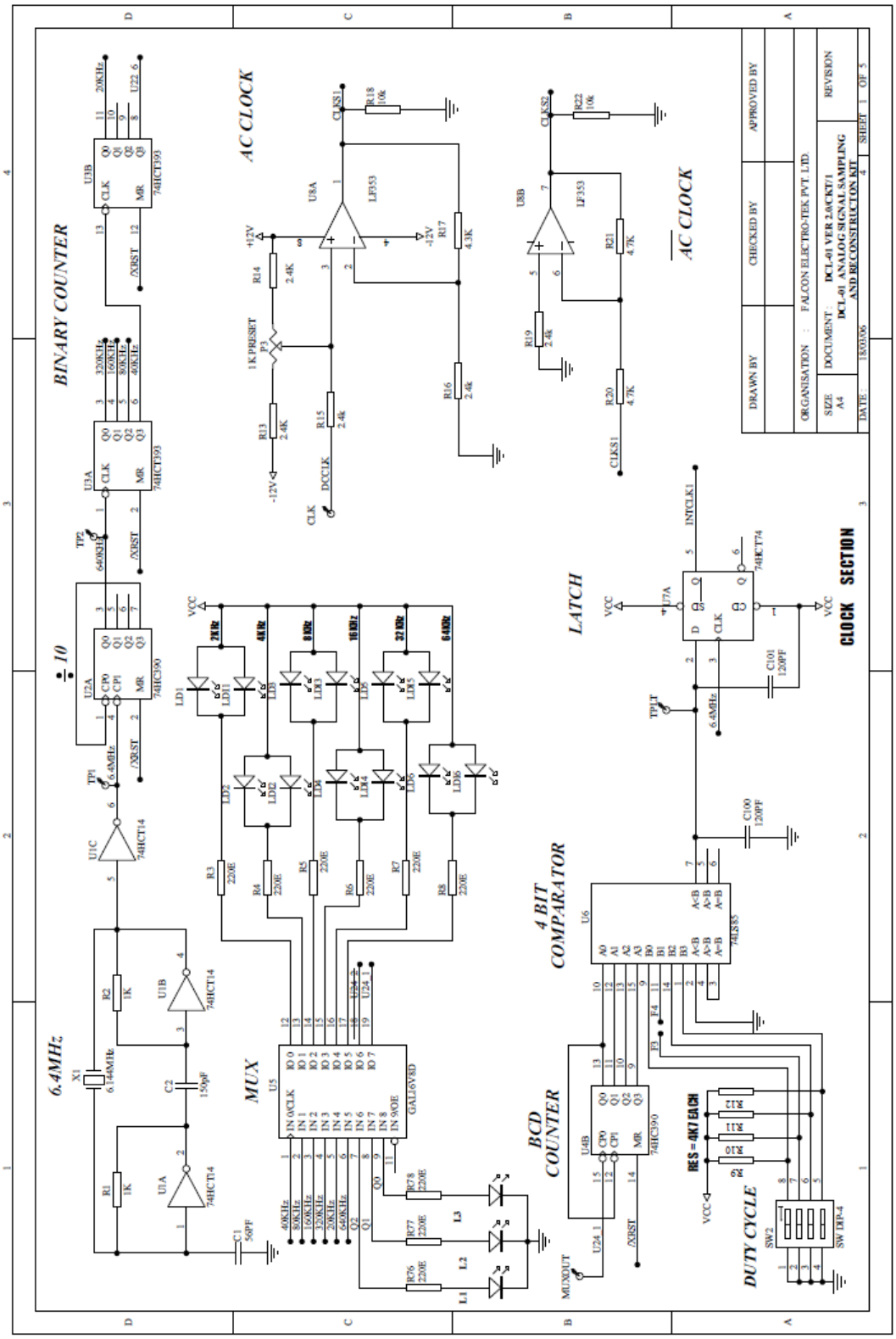
Refer to the circuit diagram as shown later in this manual sheet 5 of 5 of **DCL-01**. Two types of Filters are provided onboard, in which U19 (IC LM324) and resistors and capacitors are used to form filter circuits viz., 2^{nd} Order Low Pass Butterworth Filter and 4^{th} Order Low Pass Butterworth Filter.

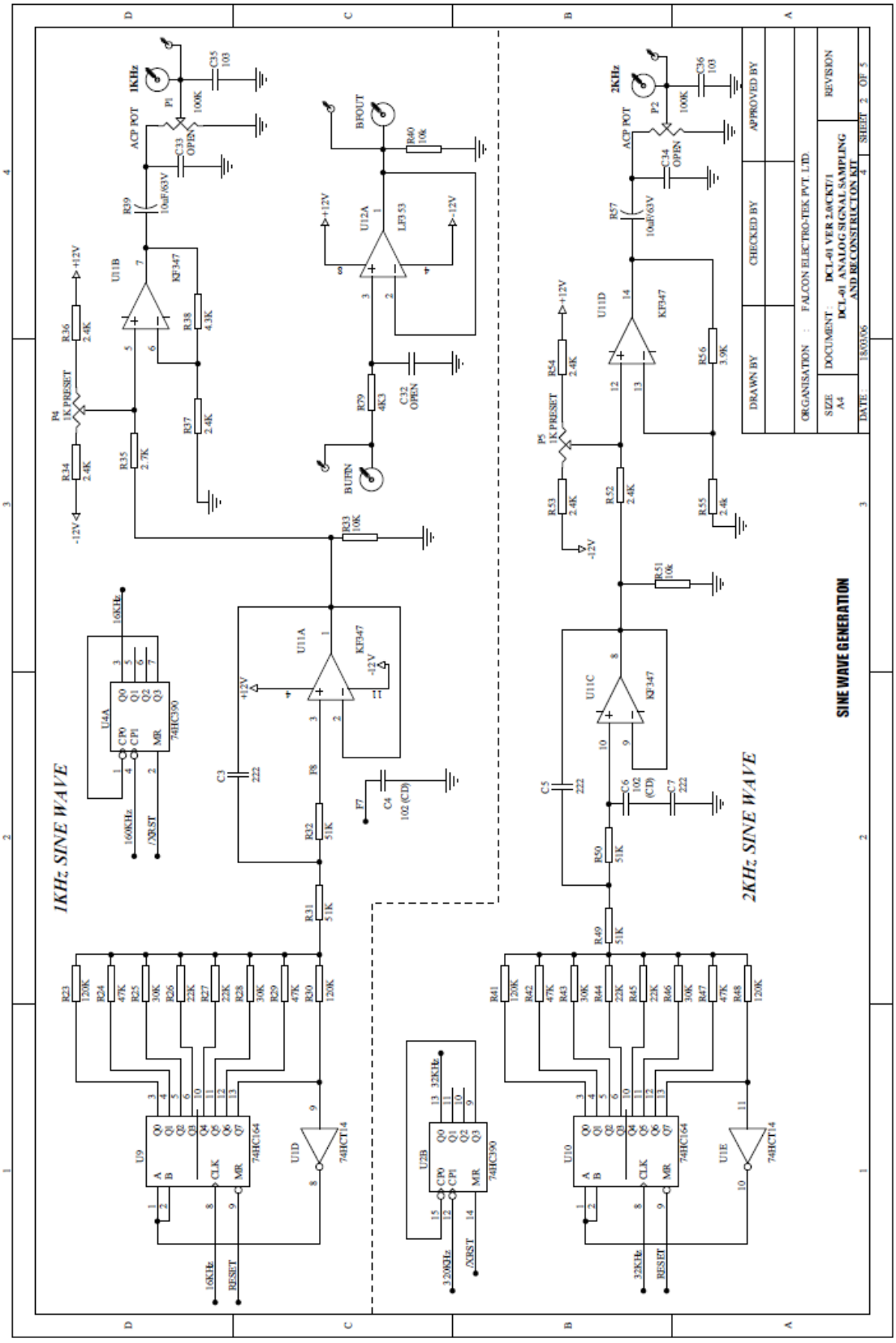
SWITCH FAULTS

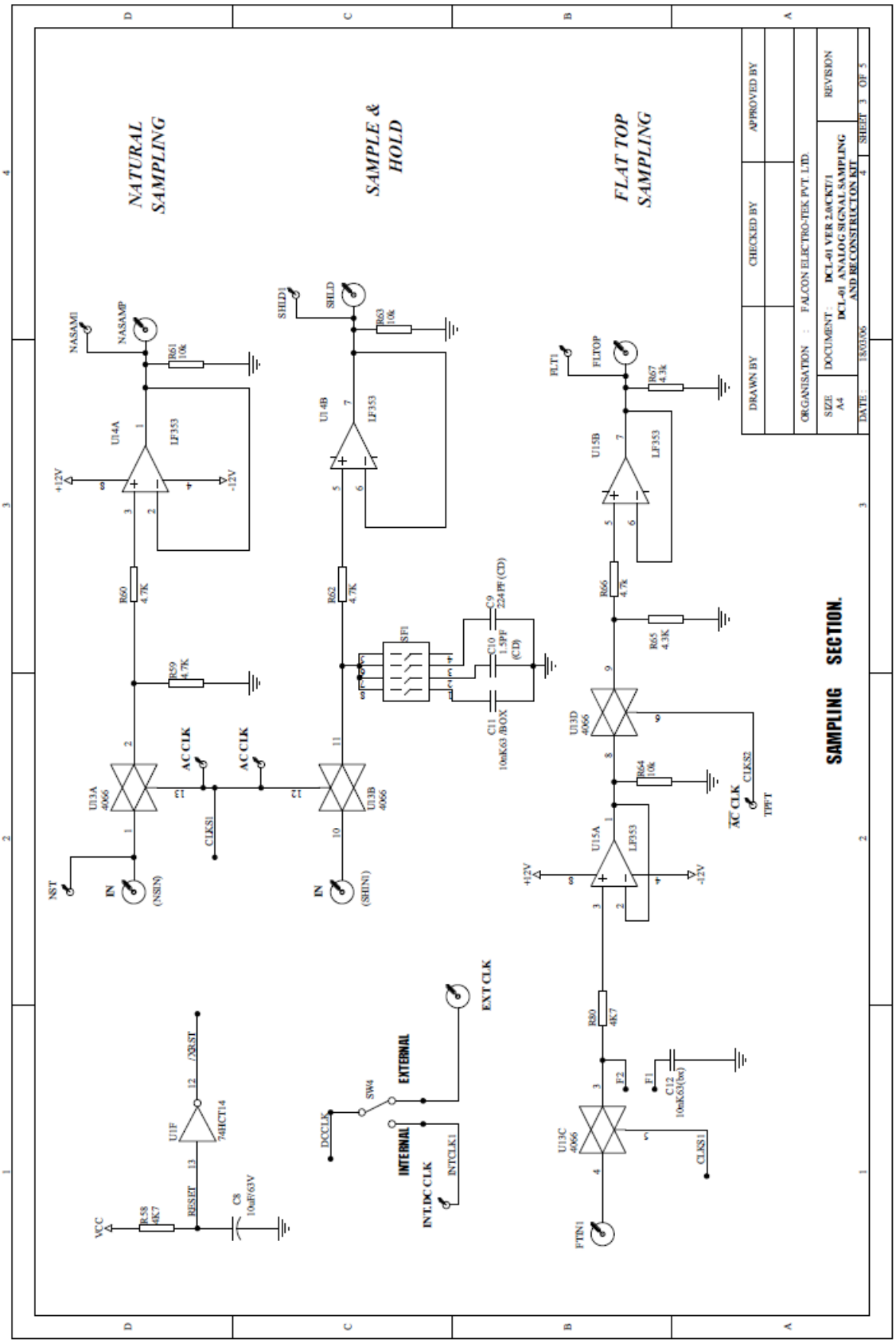
Switch fault section provides 4 switches. These switches can be used to simulate fault conditions in various parts of the circuit. The faults are normally used one at a time. To ensure that the DCL-01 kit is fully operational, all switches should be set to OFF position before use.

- Put switch **5** of **SF2** in Switch Fault section to **ON** position. This will open the capacitor C12 of the Flat Top Sampling Circuit, which makes the Flat Top sample output appears to be slant.
- Put switch **6** of **SF2** in Switch Fault section to **ON** position. This will open B1 bit from the B input (4-bit DIP switch output) of the comparator. This introduces the fault in duty cycle section. With effect, change in duty cycle for settings (10%, 40%, 50%, 80% and 90%) will not be observed as expected.
- Put switch **7** of **SF2** in Switch Fault section to **ON** position. This will open the bypass capacitor of the 2^{nd} order low pass butter-worth filter, which results in the induction of ripples at the filter output.
- Put switch **8** of **SF2** in Switch Fault section to **ON** position. This Removes the capacitor (C6) used in the generation of 1KHz sine wave, which makes the sine wave signal very distorted. The Observation can be made on this signal by changing the sampling frequencies and the duty cycle.

CIRCUIT DIAGRAM




SINE WAVE GENERATION
1KHz SINE WAVE
2KHz SINE WAVE
DRAWN BY
CHECKED BY
APPROVED BY
ORGANISATION : FALCON ELECTRO-TEK PVT LTD.
DOCUMENT : DCL-01 VER 2.0/CKT1
DCL-01 ANALOG SIGNAL SAMPLING AND RECONSTRUCTION KIT
REVISION
SIZE A4
DATE 18/01/06
SHEET 4 OF 5
ACP POT 1KHz
ACP POT 2KHz
BUTTON
74HC390
74HC164
74HCT14
KF347
LF353


NATURAL SAMPLING
SAMPLE & HOLD
FLAT TOP SAMPLING
SAMPLING SECTION.
ORGANISATION : FALCON ELECTRO-TEK PVT. LTD.
DOCUMENT : DCL-01 VER 2.0/CKT/1
DCL-01 ANALOG SIGNAL SAMPLING AND RECONSTRUCTION KIT
SIZE A4
DATE 18/03/06
SHEET 3 OF 5
REVISION
DRAWN BY
CHECKED BY
APPROVED BY
NASAMI
NASAMP
SHLDI
SHLD
FLTI
FLTOP
U14A
U14B
U15B
LF353
+12V
-12V
R60 4.7K
R59 4.7K
R61 10k
R62 4.7K
R63 10k
R66 4.7K
R65 4.3K
R67 4.3k
SF1
C9 224PF (CD)
C10 1.5PF (CD)
C11 10nK63 /BOX
U13A
U13B
U13D
4066
AC CLK
CLKS1
CLKS2
TPFT
R64 10k
U15A
R80 4K7
F1
F2
C12 10nK63(box)
U13C
CLKS1
FTIN1
NST
IN
(NSIN)
(SHIN)
R58 4K7
C8 10uF/63V
VCC
RESET
U1F
74HCT14
/RST
DCCLK
SW4
EXTERNAL
INTERNAL
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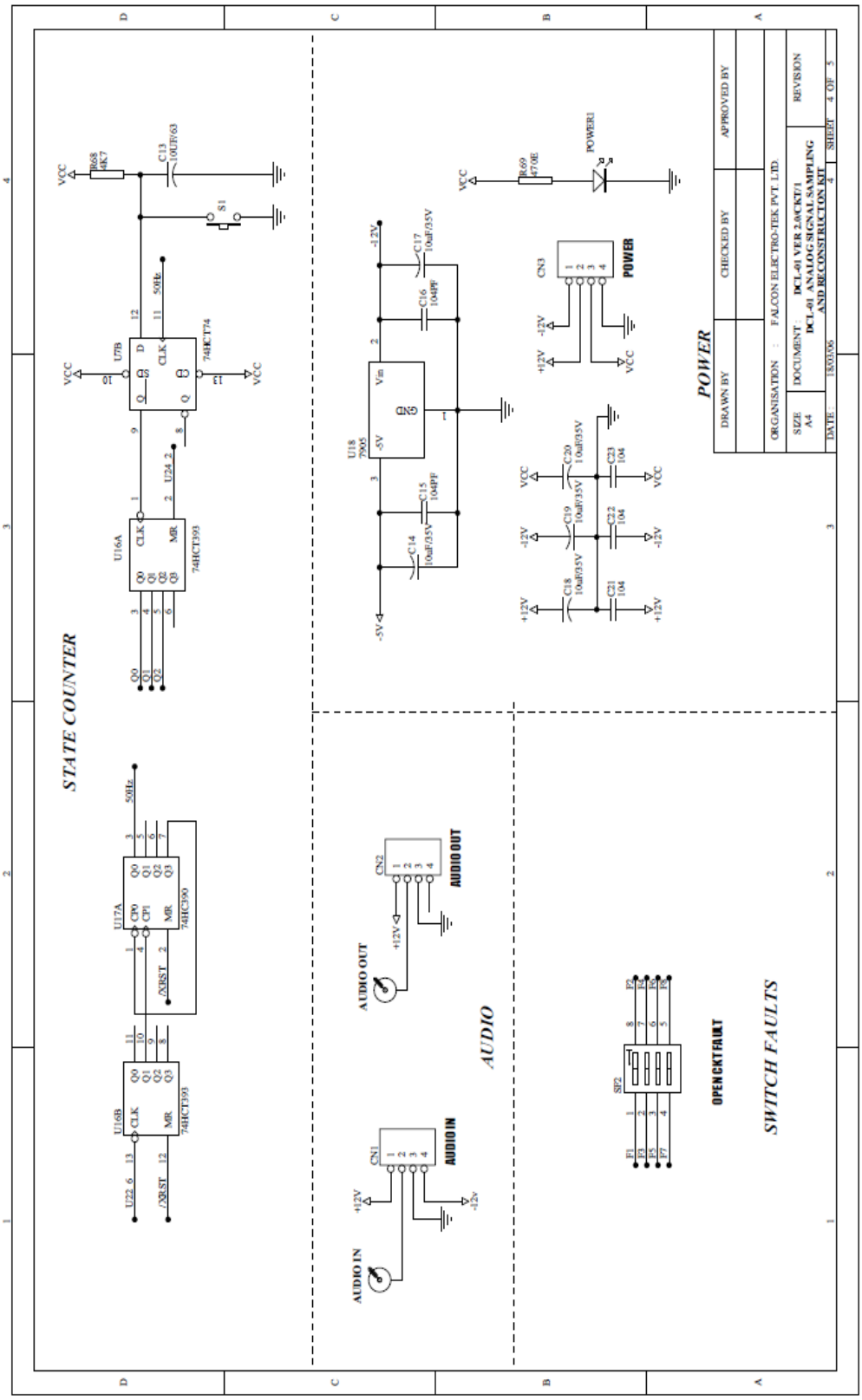
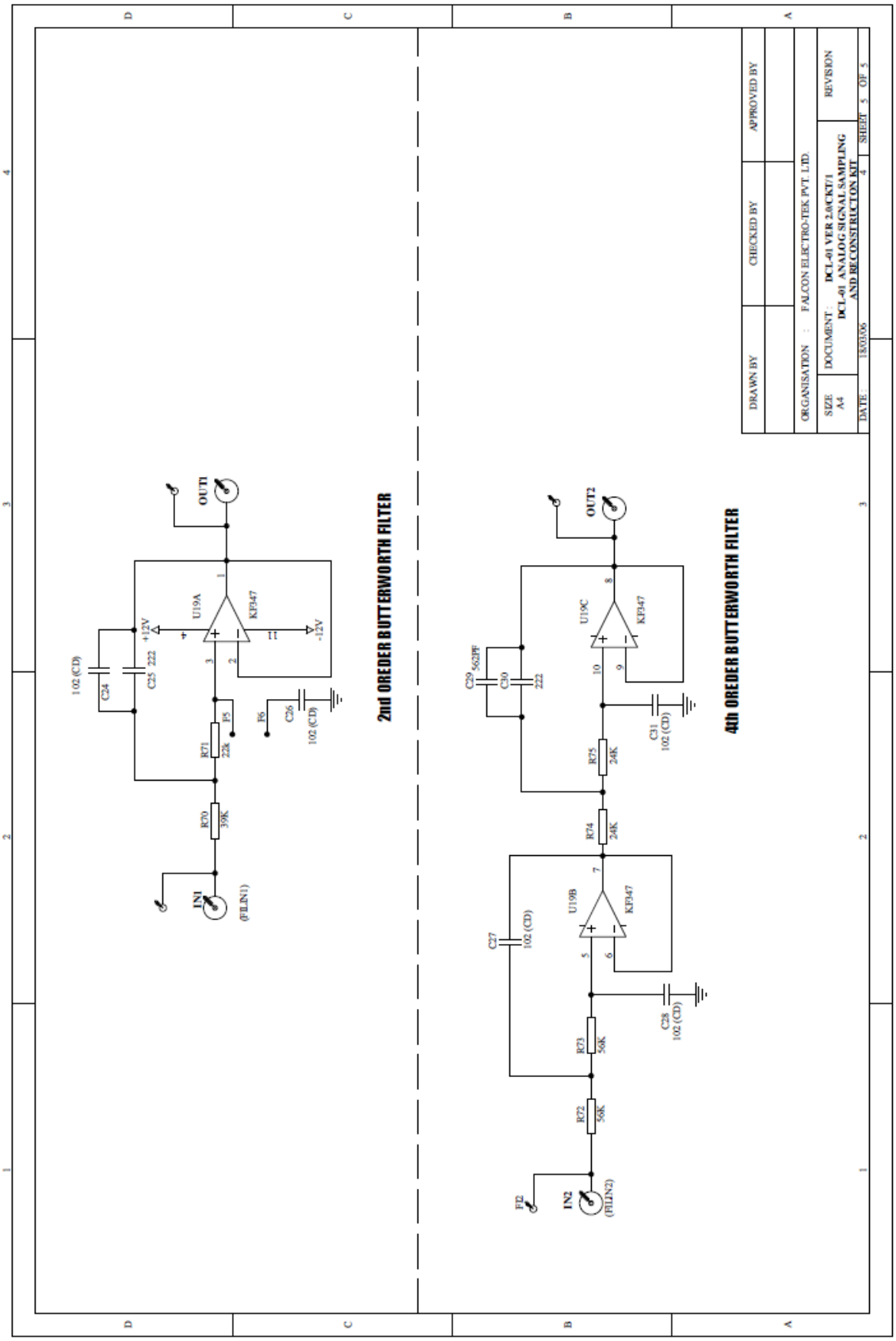
INTCLK1
EXT CLK


STATE COUNTER
AUDIO
SWITCH FAULTS
POWER
AUDIO OUT
AUDIO IN
OPEN CKT FAULT
DRAWN BY
CHECKED BY
APPROVED BY
ORGANISATION
FALCON ELECTRO-TEK PVT. LTD.
DOCUMENT
DCL-01 VER 2.0/CKT/1
DCL-01 ANALOG SIGNAL SAMPLING AND RECONSTRUCTION KIT
SIZE
A4
DATE
18/03/06
REVISION
SHEET
4 OF 5


2nd ORDER BUTTERWORTH FILTER
4th ORDER BUTTERWORTH FILTER
OUT1
OUT2
IN1
IN2
U19A
U19B
U19C
KF347
+12V
-12V
R70 39K
R71 22K
R72 56K
R73 56K
R74 24K
R75 24K
C24 102 (CD)
C25 222
C26 102 (CD)
C27 102 (CD)
C28 102 (CD)
C29 562PF
C30 222
C31 102 (CD)
J5
J6
J2
DRAWN BY
CHECKED BY
APPROVED BY
ORGANISATION : FALCON ELECTRO-TEK PVT. LTD.
DOCUMENT : DCL-01 VER 2.0/CKT/1
DCL-01 ANALOG SIGNAL SAMPLING AND RECONSTRUCTION KIT
SIZE A4
DATE 18/03/06
REVISION
SHEET 5 OF 5

EXPERIMENT NO.1

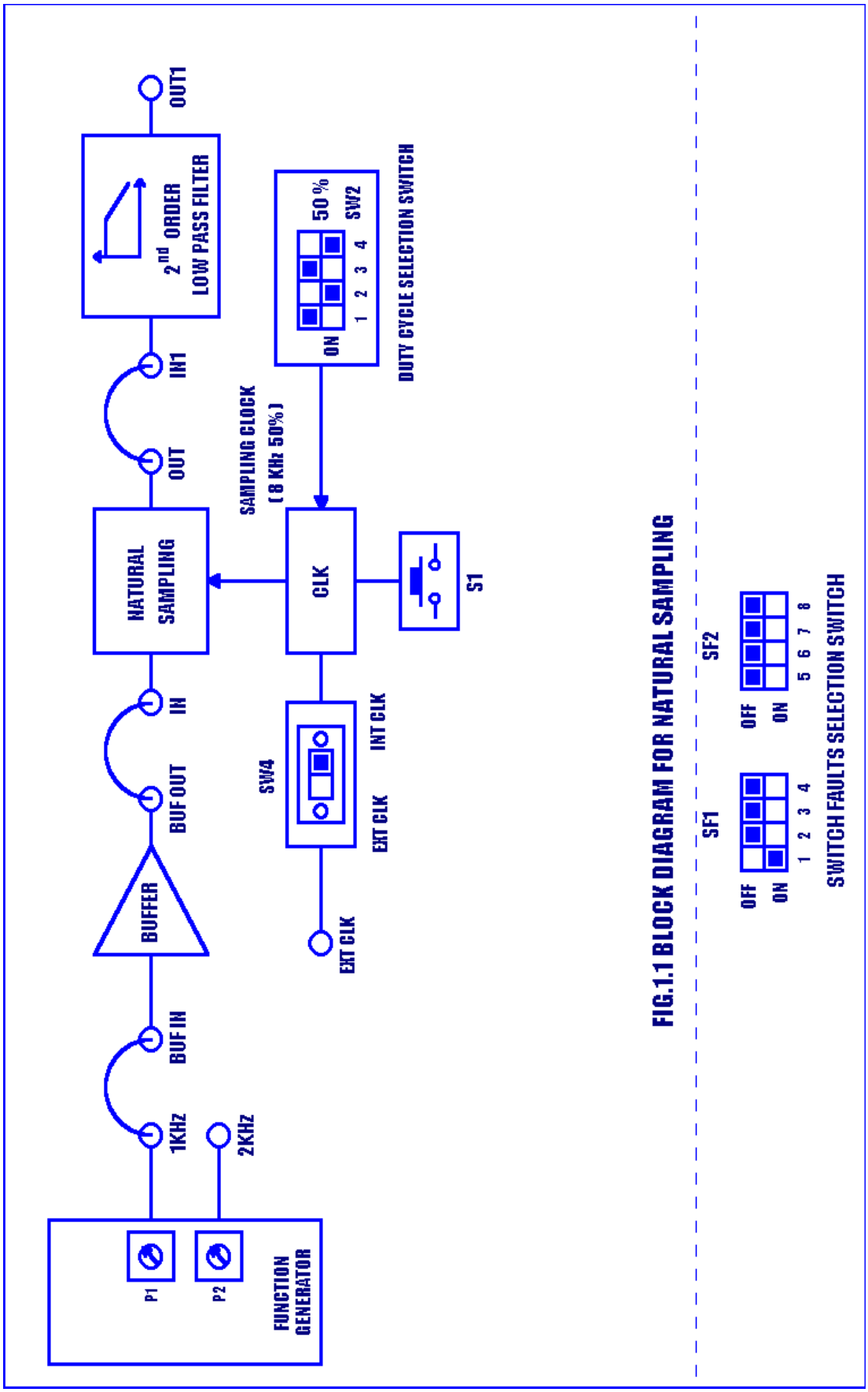


FIG.1.1 BLOCK DIAGRAM FOR NATURAL SAMPLING

EXPERIMENT NO:1

NAME

Analog Signal Sampling And Reconstruction

OBJECTIVE

To study different types of signal samplings and its reconstruction

1) Natural Sampling,
2) Sample and Hold,
3) Flat top sampling.

THEORY

The kit is used to study Analog Signal Sampling and its Reconstruction. It basically consists of functional blocks, namely Function Generator, Sampling Control Logic, Clock section, Sampling Circuitry and Filter Section.

Function Generator

This Block generates two sine wave signals of 1 KHz and 2 KHz frequency. This sine wave generation is done by feeding 16 KHz and 32 KHz clock to the shift register. The serial to parallel shift register with the resistive ladder network at the output generates 1 KHz and 2 KHz sine waves respectively by the serial shift operation. The R-C active filter suppresses the ripple and smoothness the sine wave. The unity gain amplifier buffer takes care of the impedance matching between sine wave generation and sampling circuit.

Sampling Control Logic

This unit generates two main signals used in the study of Sampling Theorem, namely the analog signals (5V pp, frequency 1KHz and 2KHz) & sampling signal of frequency 2KHz, 4KHz, 8KHz, 16KHz, 32KHz, and 64KHz.

The 6.4 MHz Crystal Oscillator generates the 6.4 MHz clock. The decade counter divides the frequency by 10 and the ripple counter generates the basic sampling frequencies from 2 KHz to 64KHz and the other control frequencies.

From among the various available sampling frequencies, required sampling frequency is selected by using the Frequency selectable switch. The selected sampling frequency is indicated by means of corresponding LED.

Clock Section

This section facilitates the user to have his choice of external or internal clock feeding to the sampling section by using a switch (SW4).

Sampling Circuitry

The unit has three parts namely, Natural Sampling Circuit, Flat top Sampling Circuit, and Sample and Hold Circuit.

The Natural sampling section takes sine wave as analog input and samples the analog input at the rate equal to the sampling signal.

For sample and hold circuit, the output is taken across a capacitor, which holds the level of the samples until the next sample arrives.
For flat top sampling clock used is inverted to that of sample & hold circuit. Output of flat top sampling circuit is pulses with flat top and top corresponds to the level of analog signal at the instant of rising edge of the clock signal.

Filter Section
Two types of Filters are provided on board, viz., 2nd Order and 4th Order Low Pass Butterworth Filter.

EQUIPMENTS

Experimenter kit DCL –01.
Connecting Chords
Power supply
20 MHz Dual Trace Oscilloscope

NOTE: Keep All the Switch Faults (Except Switch 1) In Off Position

PROCEDURE

1) Natural Sampling And Its Reconstruction

1. Refer to the Block Diagram (Fig. 1.1) & Carry out the following connections and switch settings.
2. Connect power supply in proper polarity to the kit **DCL-01** & switch it on.
3. Connect the **1 KHz**, 5Vpp Sine wave signal, generated on board; to the **BUF IN** post of the BUFFER and **BUF OUT** post of the BUFFER to the **IN** post of the Natural Sampling block by means of the Connecting chords provided.
4. Connect the sampling frequency clock in the internal mode **INT CLK** using switch **(SW4)**.
5. Using clock selector switch **(S1)** select **8 KHz** sampling frequency.
6. Using switch **SW2** select **50%** duty cycle.
7. Connect the **OUT** post of the Natural sampling block to the input **IN1** post of the 2nd Order Low Pass Butterworth Filter and take necessary observation as mentioned below. (Fig. 1.4)
8. Repeat the procedure for the 2 KHz sine wave signal as input.

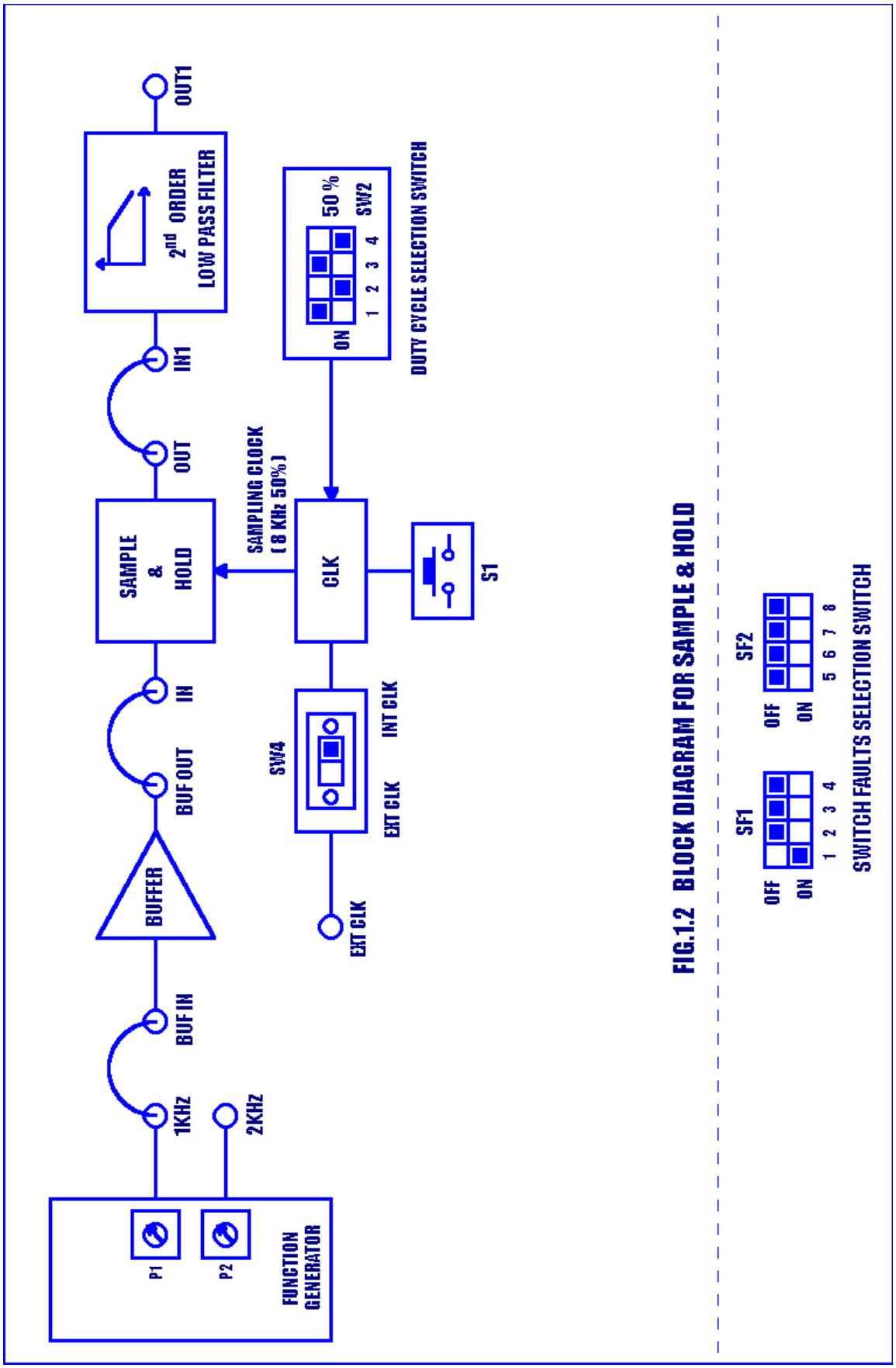


FIG.1.2 BLOCK DIAGRAM FOR SAMPLE & HOLD

OBSERVATIONS

Observe the following waveforms in order for every setting and plot it on the paper.

a. Analog Input waveform.
b. Sampling frequency waveform.
c. Natural sampling signal and its corresponding reconstructed output of 2^{nd} order Low Pass Butterworth Filter.

SWITCH FAULTS

Note: Keep the connections as per the procedure. Now switch corresponding fault switch button in ON condition & observe the different effect on the output. The faults are normally used one at a time.

- Put switch **6** of **SF2** in Switch Fault section to **ON** position. This will open B1 bit from the B input (4-bit DIP switch output) of the comparator. This introduces the fault in duty cycle section. With effect, change in duty cycle for settings (10%, 40%, 50%, 80% and 90%) will not be observed as expected.
- Put switch **7** of **SF2** in Switch Fault section to **ON** position. This will open the bypass capacitor of the 2^{nd} order low pass butter-worth filter, which results in the induction of ripples at the filter output.
- Put switch **8** of **SF2** in Switch Fault section to **ON** position. This Removes the capacitor (C6) used in the generation of 1 KHz sine wave. Which makes the sine wave signal very distorted. The Observation can be made on this signal by changing the sampling frequencies and the duty cycle.

PROCEDURE

2) Sample And Hold And Its Reconstruction

1. Refer to the Block Diagram (Fig. 1.2) & Carry out the following connections and switch settings.
2. Connect power supply in proper polarity to the kit **DCL-01** & switch it on.
3. Connect the **1 KHz**, 5Vpp Sine wave signal, generated onboard, to the **BUF IN** post of the BUFFER and the **BUF OUT** post of the BUFFER to the **IN** post of the Sample and Hold Block by means of the Connecting chords provided.
4. Connect the sampling frequency clock in the internal mode **INT CLK** using switch **(SW4)**.
5. Using clock selector switch **SW1** select **8 KHz** sampling frequency.
6. Using switch **SW2** select **50%** duty cycle.
7. Connect the **OUT** post of the Sample and Hold block to the input **IN 1** post of the 2^{nd} Order Low Pass Butterworth Filter and take necessary observation as mentioned below. (Fig. 1.5)
8. Repeat the procedure for the 2 KHz sine wave signal as input.

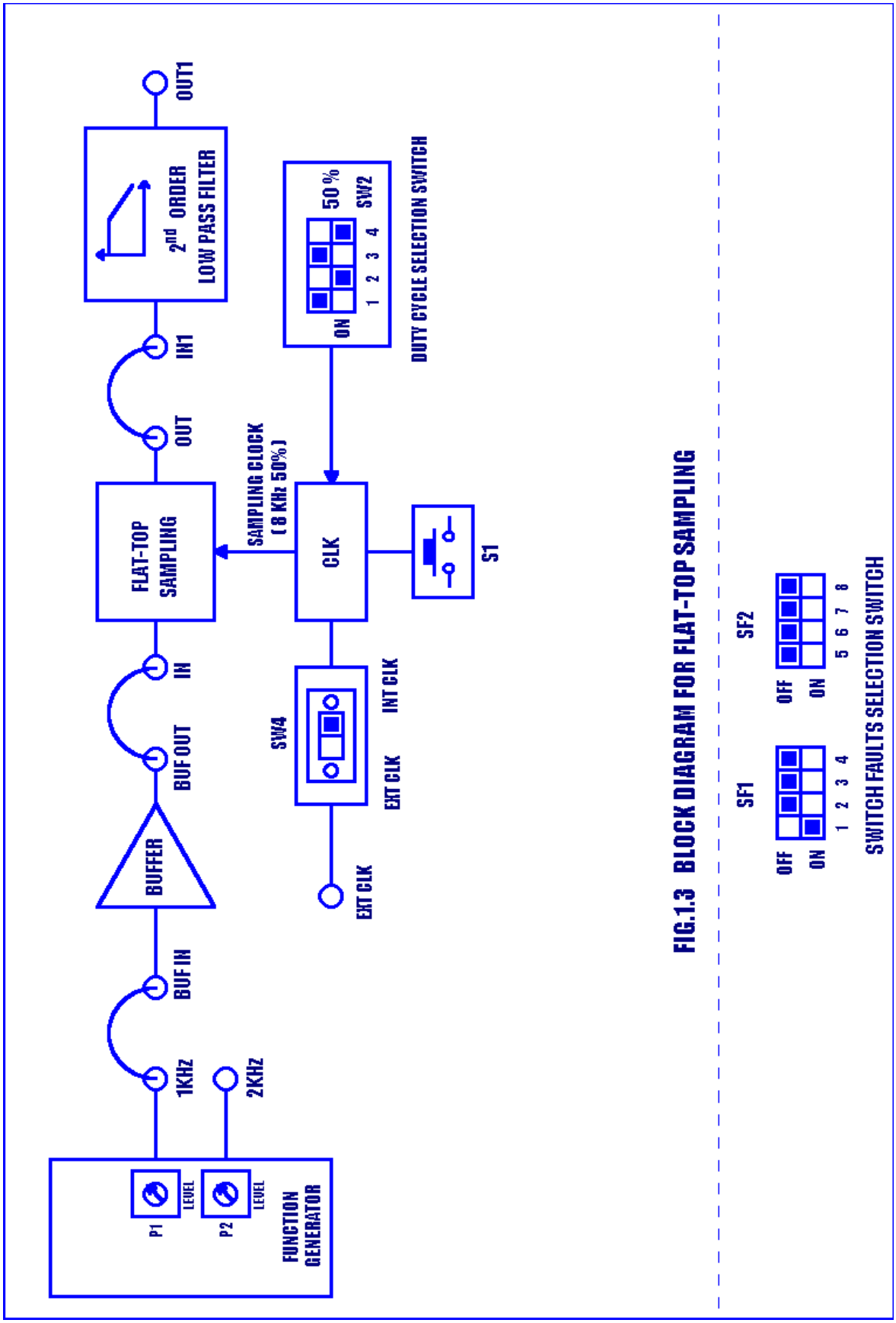


FIG.1.3 BLOCK DIAGRAM FOR FLAT-TOP SAMPLING

OBSERVATIONS

Observe the following waveforms in order for every setting and plot it on the paper.

A) 1 KHz Analog Input waveform
B) Sampling frequency waveform.
C) Sample and hold signal and its corresponding reconstructed output of 2^{nd} order Low Pass Butterworth Filter.

By changing the position of the switch in the **SF1** you are changing the Capacitance value of the Sample and Hold circuit, you can find the variation accordingly at the output of the Sample and Hold circuit.

- Put switch **2** of **SF1** in Switch Fault section to **ON** position, the capacitor C10 (1.5pF) is at the output of sample and hold circuit.
- Put switch **3** of **SF1** in Switch Fault section to **ON** position, the capacitor C9 (0.22μF) is at the output of sample and hold circuit.

SWITCH FAULTS

Note: Keep the connections as per the procedure. Now switch corresponding fault switch button in ON condition & observe the different effect on the output. The faults are normally used one at a time.

- Put switch **6** of **SF2** in Switch Fault section to **ON** position. This will open B1 bit from the B input (4-bit DIP switch output) of the comparator. This introduces the fault in duty cycle section. With effect, change in duty cycle for settings (10%, 40%, 50%, 80% and 90%) will not be observed as expected.
- Put switch **7** of **SF2** in Switch Fault section to **ON** position. This will open the bypass capacitor of the 2^{nd} order low pass butter-worth filter, which results in the induction of ripples at the filter output.
- Put switch **8** of **SF2** in Switch Fault section to **ON** position. This Removes the capacitor (C6) used in the generation of 1KHz sine wave. Which makes the sine wave signal very distorted. The Observation can be made on this signal by changing the sampling frequencies and the duty cycle.

PROCEDURE

4) Flat Top Sampling And Its Reconstruction

1. Refer to the Block Diagram (Fig. 1.3) & Carry out the following connections and switch settings.
2. Connect power supply in proper polarity to the kit **DCL-01** & switch it on.
3. Connect the **1 KHz**, 5Vpp Sine wave signal, generated onboard to the **BUF IN** post of the Buffer and the **BUF OUT** post of the Buffer to the **IN** post of the Flat Top Sampling block by means of the Connecting chords provided.
4. Connect the sampling frequency clock in the internal mode **INT CLK** using switch **(SW4)**.
5. Using clock selector switch **S1** select **8 KHz** sampling frequency.
6. Using switch **SW2** select **50%** duty cycle.

7. Connect the **OUT** post of the flat top sampling block to the input **IN 1** of the 2nd Order Low Pass Butterworth Filter and take necessary observation as mentioned below. (Fig. 1.6)
8. Repeat the procedure for the 2 KHz sine wave signal as input.

OBSERVATIONS

Observe the following waveforms in order for every setting and plot it on the paper.

a. Analog Input waveform
b. Sampling frequency waveform
c. Flat Top signal and its corresponding reconstructed output of 2nd order Low Pass Butterworth Filter

In this manner we observe all the three types of sampling, which can be compared with the waveforms at the end of this experiment.

We observe that, during the ON time of sampling frequency the analog signal is transmitted. During the OFF time, the sample output signal drops towards zero. Whereas for Sampled and Hold output, the signal maintains the voltage level i.e. the sample is held at last sampled value until next sample arrives. For flat top sampling first switching portion from sample & hold signal is dropped and next switching portion is taken as pulse output, i.e. only hold portion from sample & hold signal is taken at flat top sampling output.

SWITCH FAULTS

Note: Keep the connections as per the procedure. Now switch corresponding fault switch button in ON condition & observe the different effect on the output. The faults are normally used one at a time.

- Put switch **5** of **SF2** in Switch Fault section to **ON** position. This will open the capacitor C12 of the Flat Top Sampling Circuit, which makes the Flat Top sample output appears to be slant.
- Put switch **6** of **SF2** in Switch Fault section to **ON** position. This will open B1 bit from the B input (4-bit DIP switch output) of the comparator. This introduces the fault in duty cycle section. With effect, change in duty cycle for settings (10%, 40%, 50%, 80% and 90%) will not be observed as expected.
- Put switch **7** of **SF2** in Switch Fault section to **ON** position. This will open the bypass capacitor of the 2nd order low pass butterworth filter, which results in the induction of ripples at the filter output.
- Put switch **8** of **SF2** in Switch Fault section to **ON** position. This Removes the capacitor (C6) used in the generation of 1KHz sine wave. Which makes the sine wave signal very distorted. The Observation can be made on this signal by changing the sampling frequencies and the duty cycle**.**

CONCLUSION

Comparing the reconstructed output of 2nd order Low Pass Butterworth Filter for all the three types of sampling, it is observed that the output of the sample and hold is the best as compared to the output of natural sampling and the output of the flat top sampling.

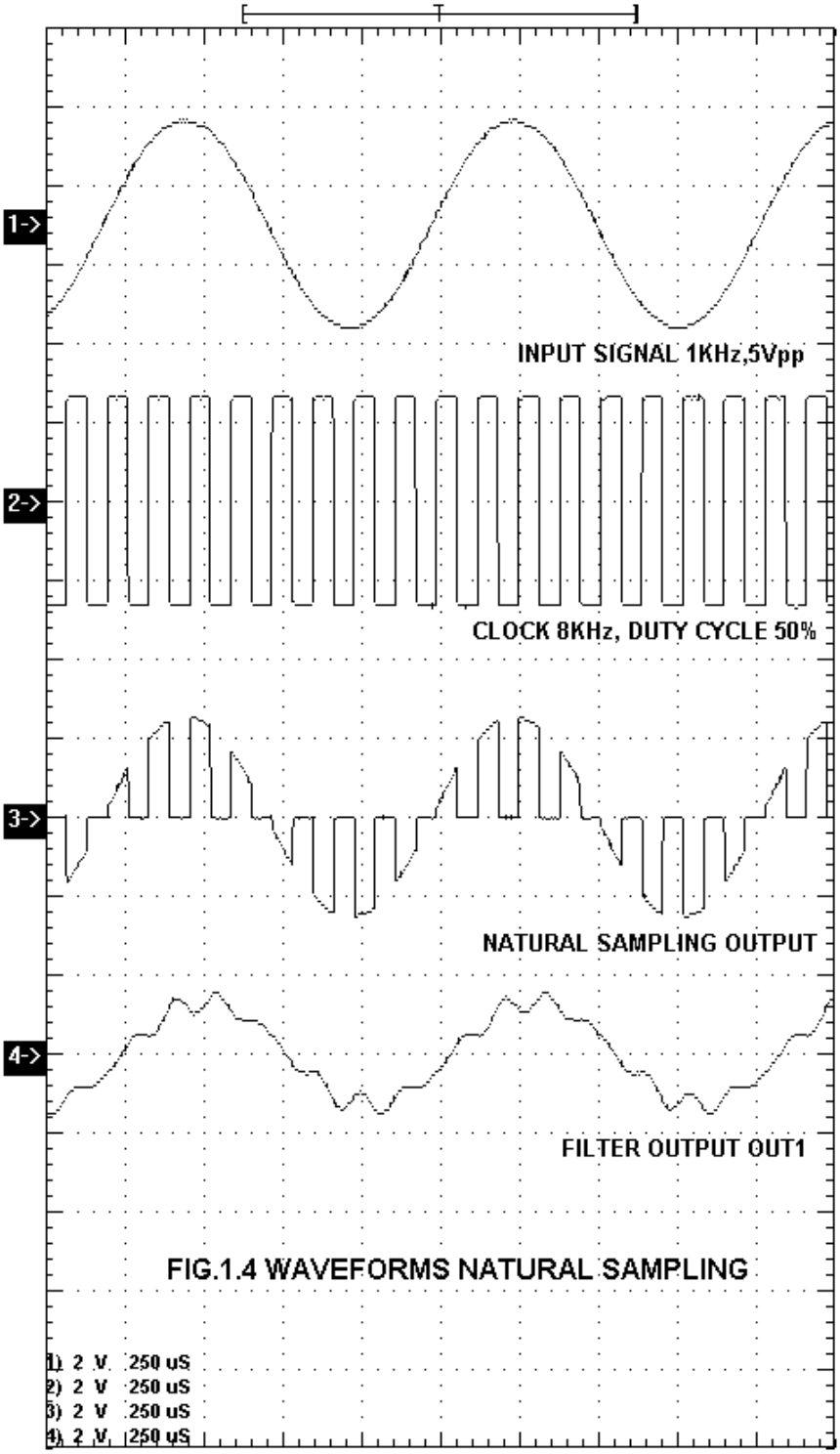


FIG.1.4 WAVEFORMS NATURAL SAMPLING

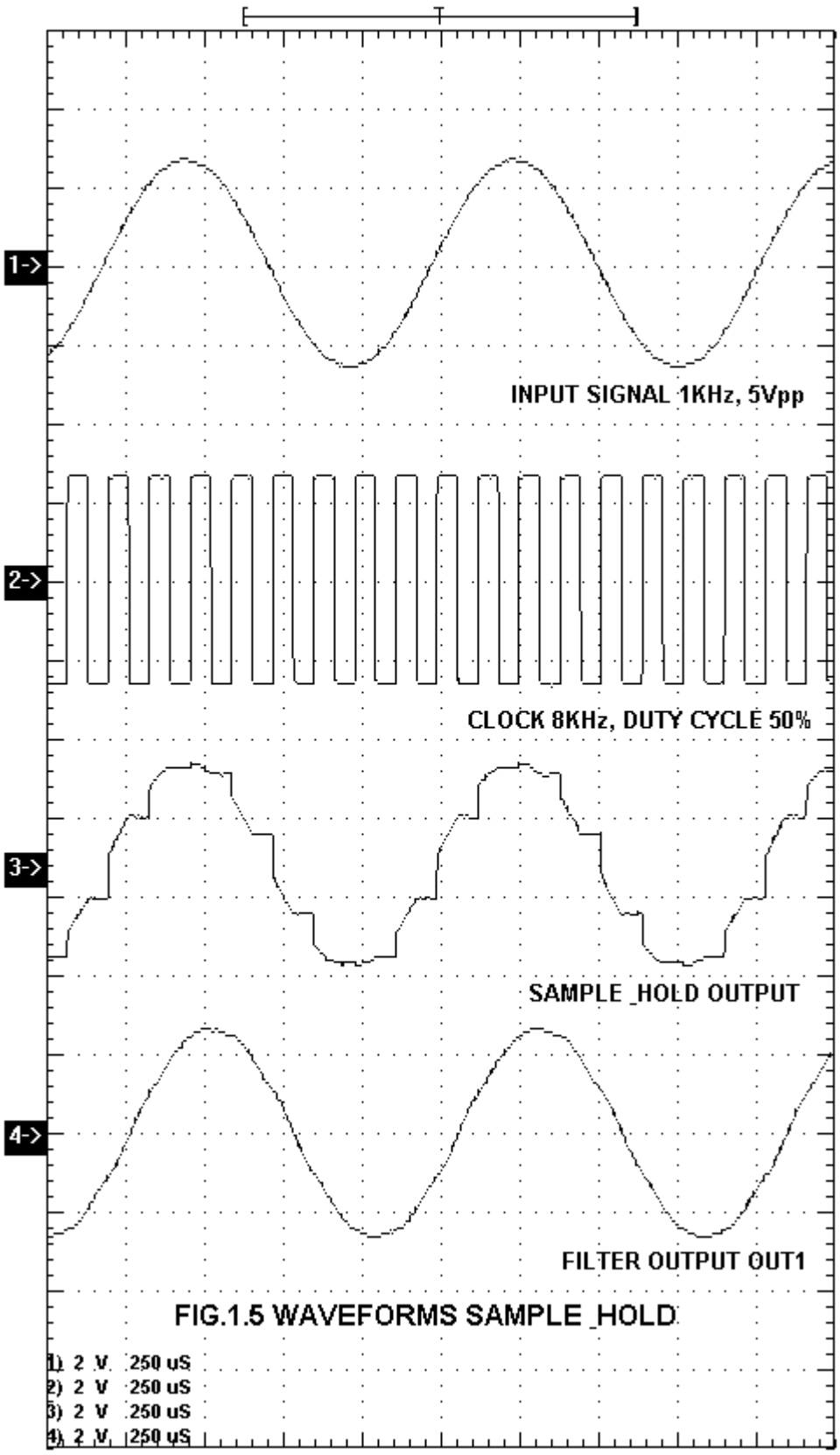


FIG.1.5 WAVEFORMS SAMPLE _HOLD

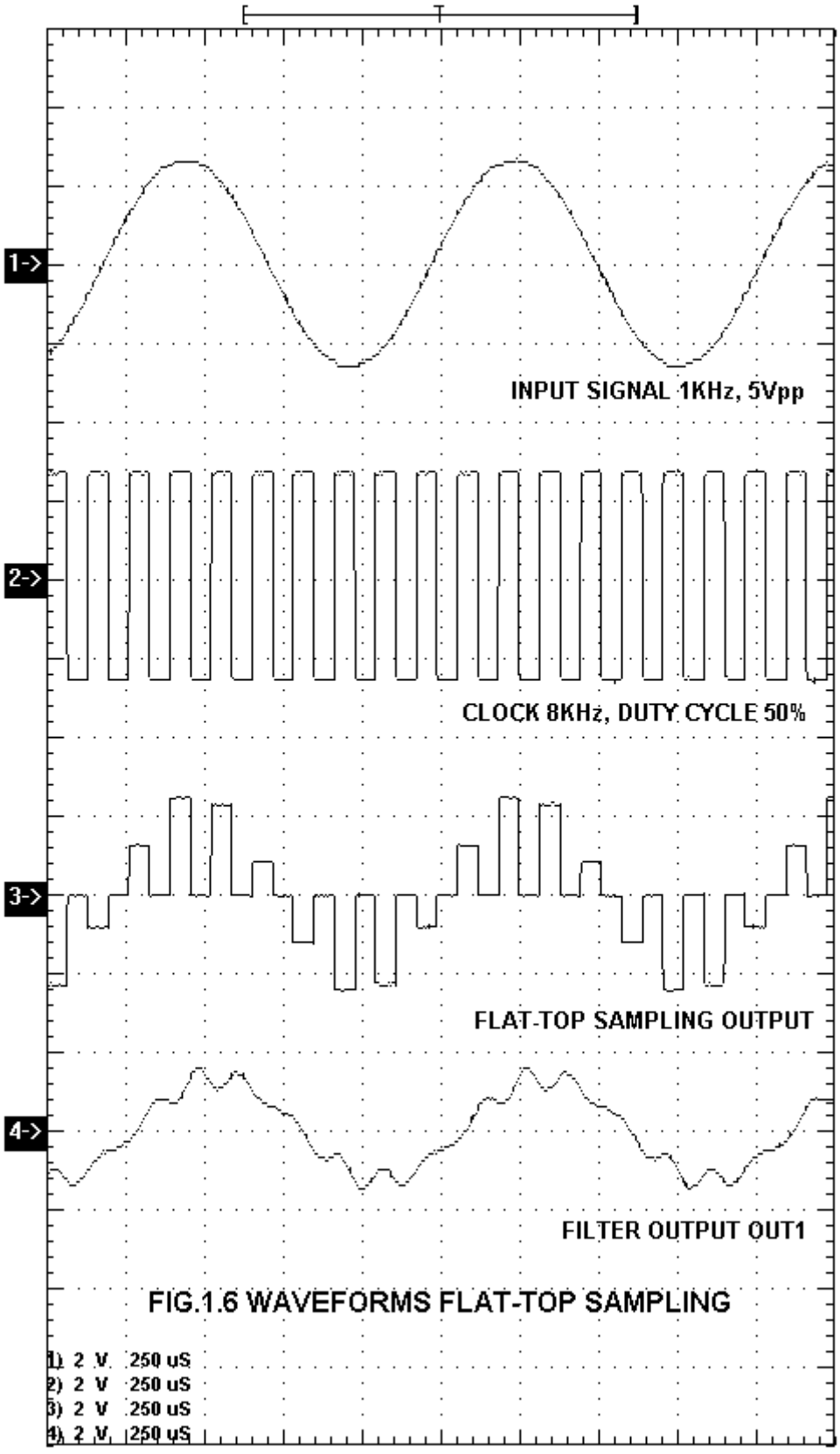


FIG.1.6 WAVEFORMS FLAT-TOP SAMPLING

EXPERIMENT NO.2

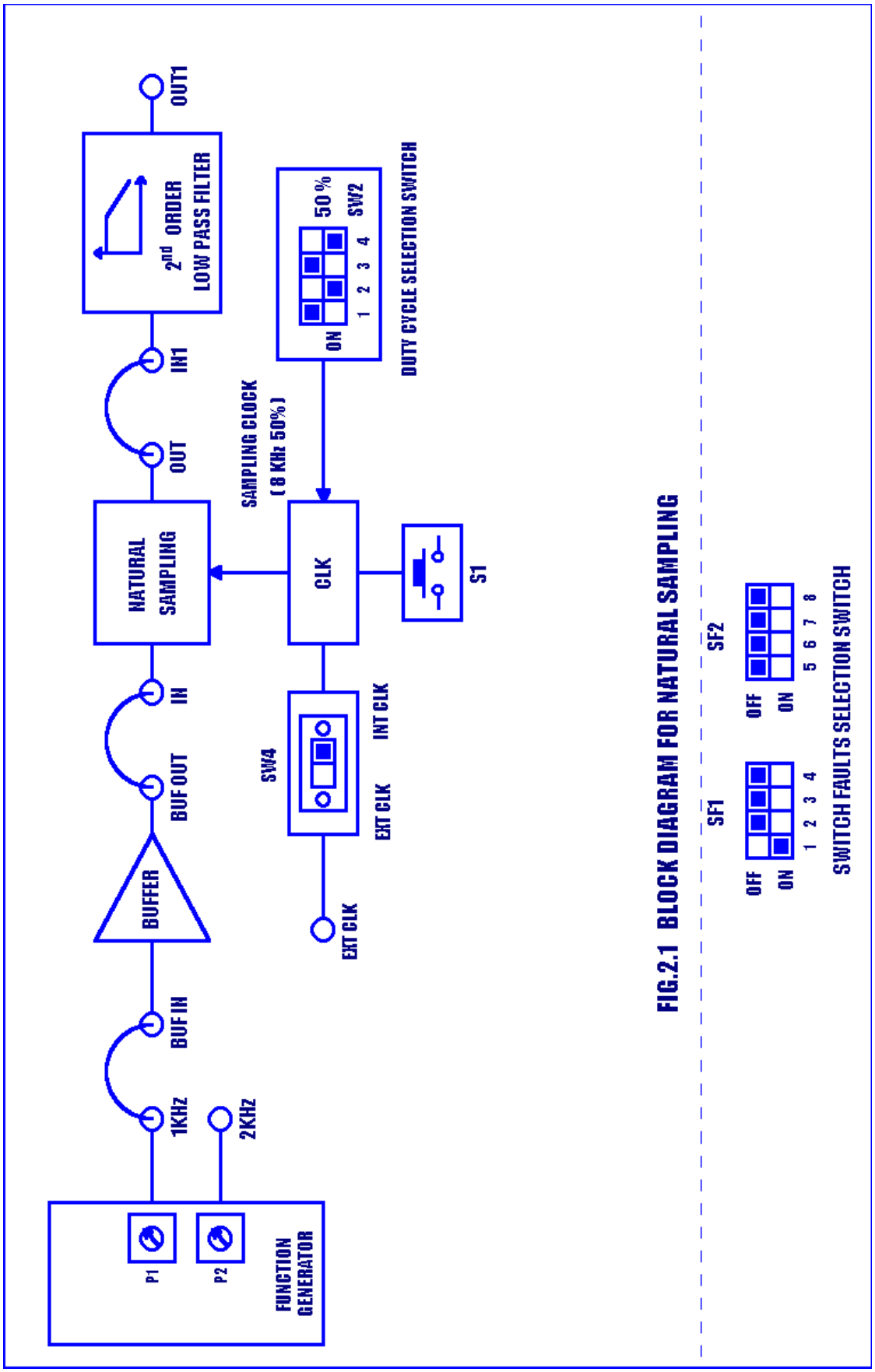


FIG.2.1 BLOCK DIAGRAM FOR NATURAL SAMPLING

EXPERIMENT NO: 2

NAME

To Study Effect of Different Sampling Frequencies

OBJECTIVE

To study the effect of different sampling frequencies on the reconstructed signal

THEORY

Sampling Frequency
The 6.4 MHz Crystal oscillator generates the 6.4 MHz clock. The decade counter divides the frequency by 10 and the ripple counter generates the basic sampling frequencies 640 KHz to 20 KHz and the other control frequencies.
The basic sampling frequency is given to a multiplexer. For each “Press” on the frequency select switch, the output of the state counter increases by one and it counts from 000 to 101. As the state counter counts from 000 to 101, the corresponding input of the mux is switched to the output. As soon as the count reaches 110, the output of the 3 to 8 decoder resets the state counter and the whole cycle repeats. Also LED connected to the output of the decoder is switched ON, which indicates the sampling frequency selected.

EQUIPMENTS

Experimenter kit DCL –01.
Connecting Chords
Power supply
20 MHz Dual Trace Oscilloscope

NOTE: Keep All The Switch Faults (Except Switch 1) In Off Position

PROCEDURE

1. Refer to the Block Diagram (Fig. 2.1) & Carry out the following connections and switch settings.
2. Connect power supply in proper polarity to the kit **DCL-01** & switch it on.
3. Connect the **1 KHz**, 5Vpp Sine wave signal, generated on-board, to the **BUF IN** post of the BUFFER and the **BUF OUT** post of the BUFFER to the **IN** post of Natural sampling block by means of the Connecting chords provided.
4. Connect the sampling frequency signal in the internal mode **INT CLK** using Switch **(SW4)**.
5. Using switch **SW2** select **50%** duty cycle.

6. Connect the Sampled Output **OUT** to the input of the **IN 1** post of 2nd Order Low Pass Butterworth Filter.
7. Using clock selectors switch **S1**, select desired sampling frequency. The sampling frequency selected is indicated by the LED.
8. Take observation as mentioned below for various sampling frequencies: 64 KHz, 32 KHz, 16 KHz, 8 KHz, 4 KHz, and 2 KHz.
9. Similarly repeat the procedure for sample & hold circuit and flat top sample circuit.
10. Also observe waveforms by applying onboard 2 KHz sine wave signal.

OBSERVATIONS

Observe the following waveforms in order for every setting and plot it on the paper.

- Analog Input waveform.
- Sampling frequency (2 KHz) waveform.
- Natural Sampled Signal and corresponding reconstructed output of 2^{nd} order Low Pass Butterworth Filter. (Fig. 2.2)
- Sample and Hold signal output and corresponding reconstructed output of 2^{nd} order Low Pass Butterworth Filter. (Fig. 2.3)
- Flat top sample signal output and corresponding reconstructed output of 2^{nd} order Low Pass Butterworth Filter. (Fig. 2.4)
- Sampling frequency (8 KHz) waveform.
- Natural Sampled Signal and corresponding reconstructed output of 2^{nd} order Low Pass Butterworth Filter. (Fig. 2.5)
- Sample and Hold signal output and corresponding reconstructed output of 2^{nd} order Low Pass Butterworth Filter. (Fig. 2.6)
- Flat top sample signal output and corresponding reconstructed output of 2^{nd} order Low Pass Butterworth Filter. (Fig. 2.7)

SWITCH FAULTS

Note: Keep the connections as per the procedure. Now switch corresponding fault switch button in ON condition & observe the different effect on the output. The faults are normally used one at a time.

- Put switch **6** of **SF2** in Switch Fault section to **ON** position. This will open B1 bit from the B input (4-bit DIP switch output) of the comparator. This introduces the fault in duty cycle section. With effect, change in duty cycle for settings (10%, 40%, 50%, 80% and 90%) will not be observed as expected.
- Put switch **7** of **SF2** in Switch Fault section to **ON** position. This will open the bypass capacitor of the 2^{nd} order low pass butter-worth filter, which results in the induction of ripples at the filter output.
- Put switch **8** of **SF2** in Switch Fault section to **ON** position. This Removes the capacitor (C6) used in the generation of 1 KHz sine wave. Which makes the sine wave signal very distorted. The Observation can be made on this signal by changing the sampling frequencies and the duty cycle.

CONCLUSION

From the above observations we conclude that as the sampling frequency is increased, the reconstructed output is less distorted and almost original signal is reconstructed.
For a sampling frequency of 2KHz, only 2 samples of the 1KHz signal are taken, whereas that for a sampling frequency of 8KHz, 8 samples of 1KHz signal is taken. Hence, as the number of samples taken of the signal increases, the distortion of the reconstructed signal decreases
As per the Nyquist Criterion at least two samples are required for the reconstruction of the signal. If the Nyquist Criterion is not satisfied, or if the signal is not band-limited, then spectral overlap, called “aliasing” occurs, causing higher frequencies to show up at lower frequencies in the recovered message, and specially in voice transmission intelligibility is seriously degraded Thus, universally for the voice band (300Hz to 3300Hz), the sampling frequency used is 8KHz, which satisfies the Nyquist Criterion.

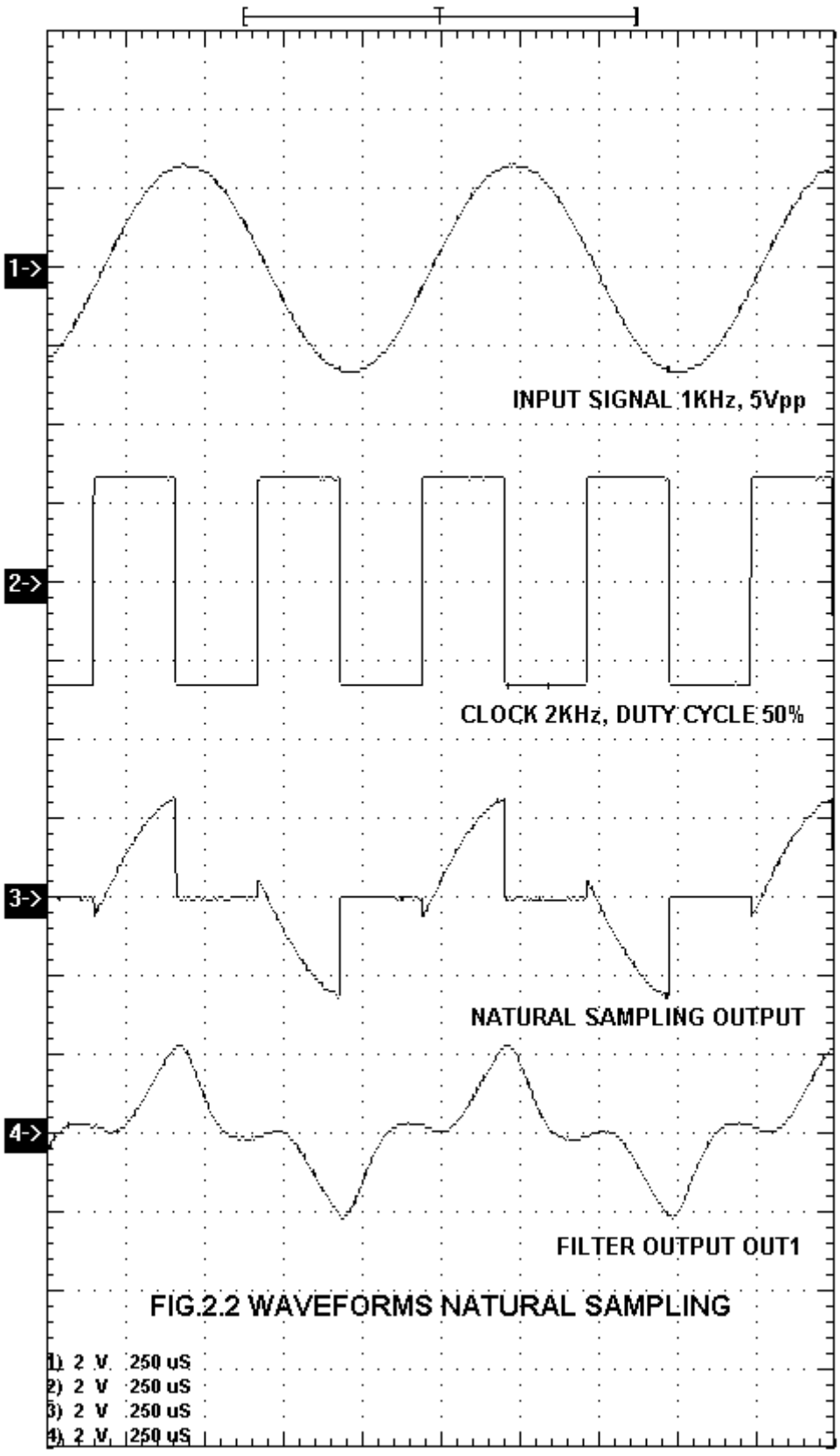


FIG.2.2 WAVEFORMS NATURAL SAMPLING

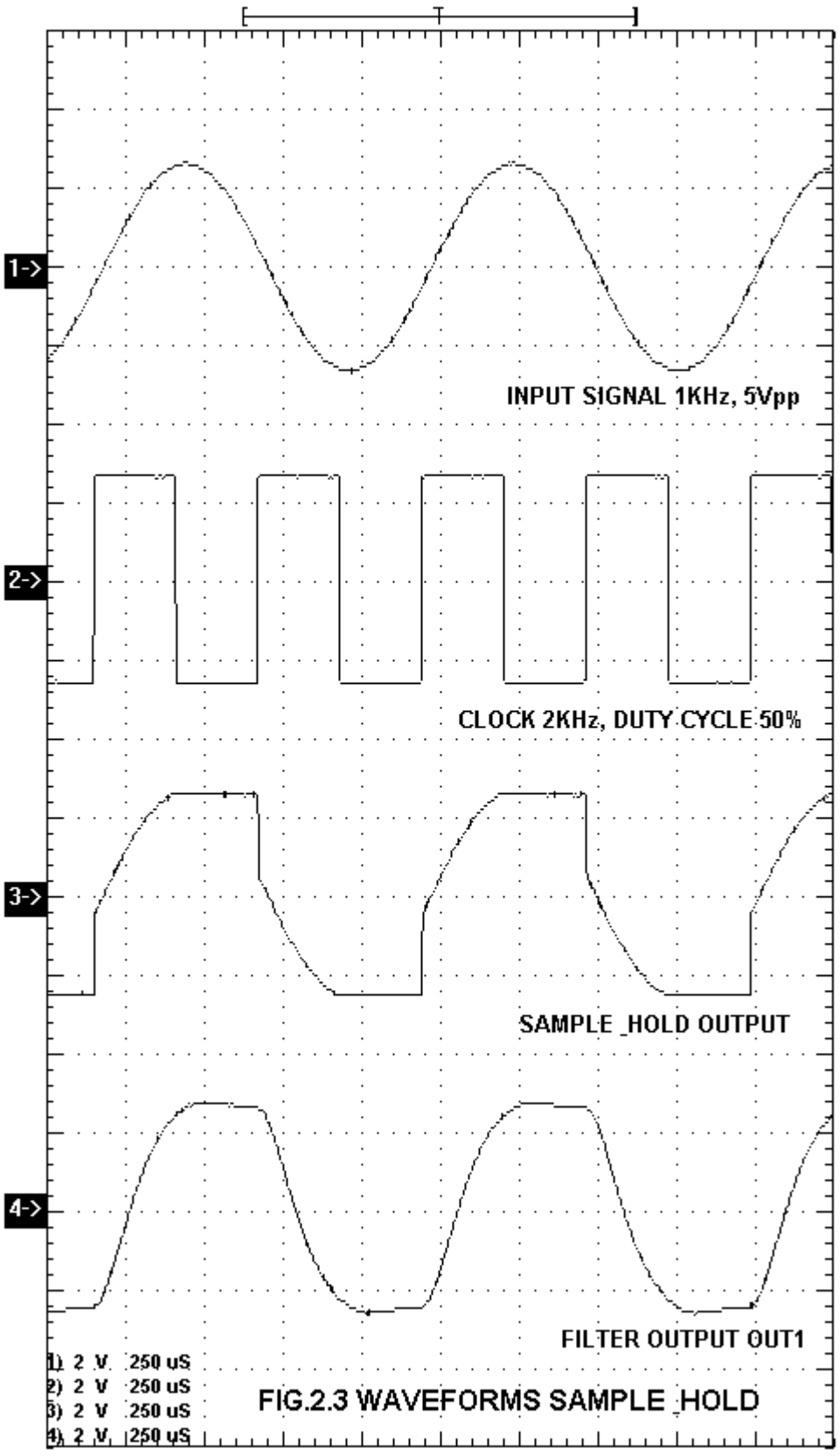


FIG.2.3 WAVEFORMS SAMPLE _HOLD

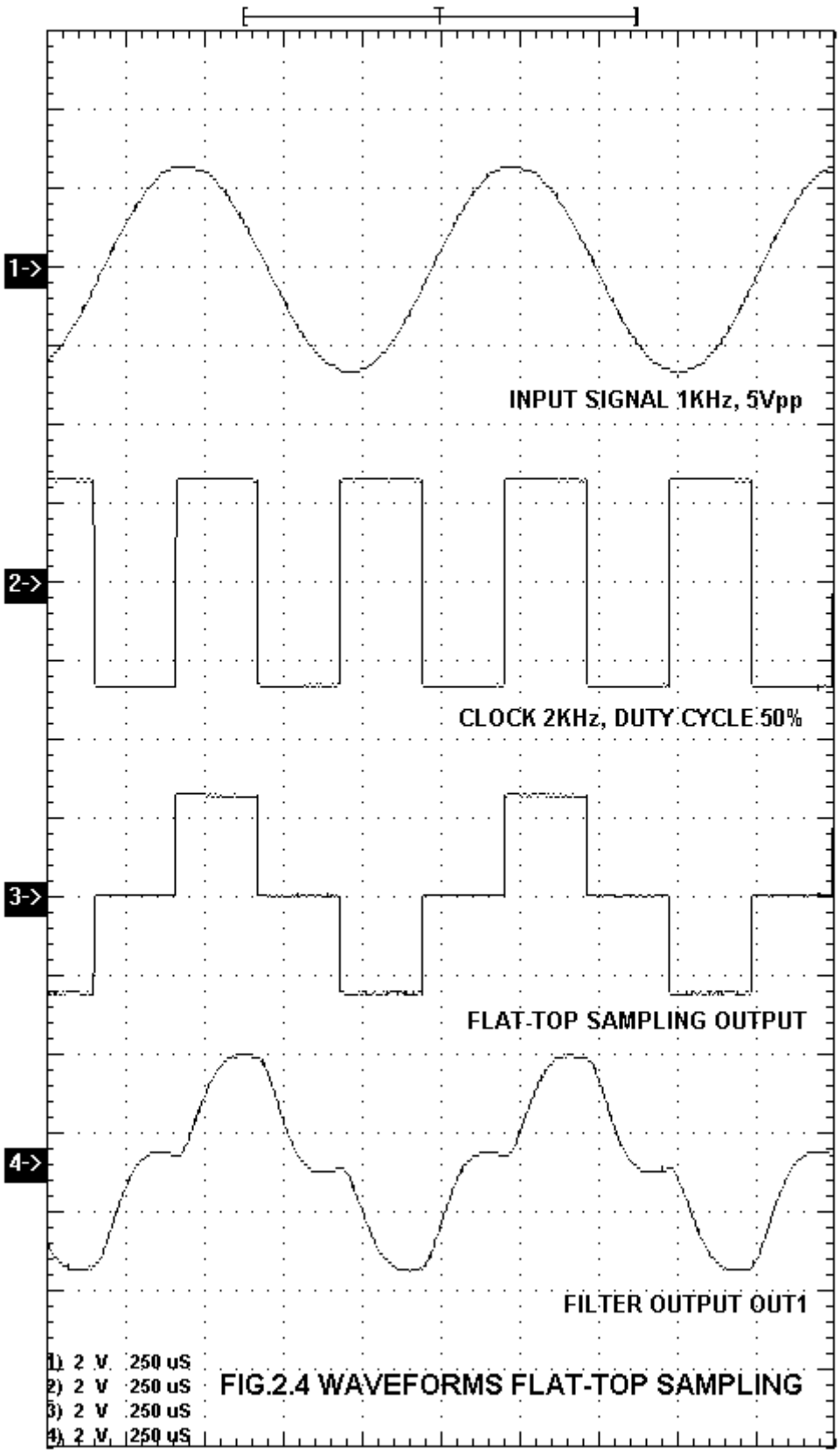


FIG.2.4 WAVEFORMS FLAT-TOP SAMPLING

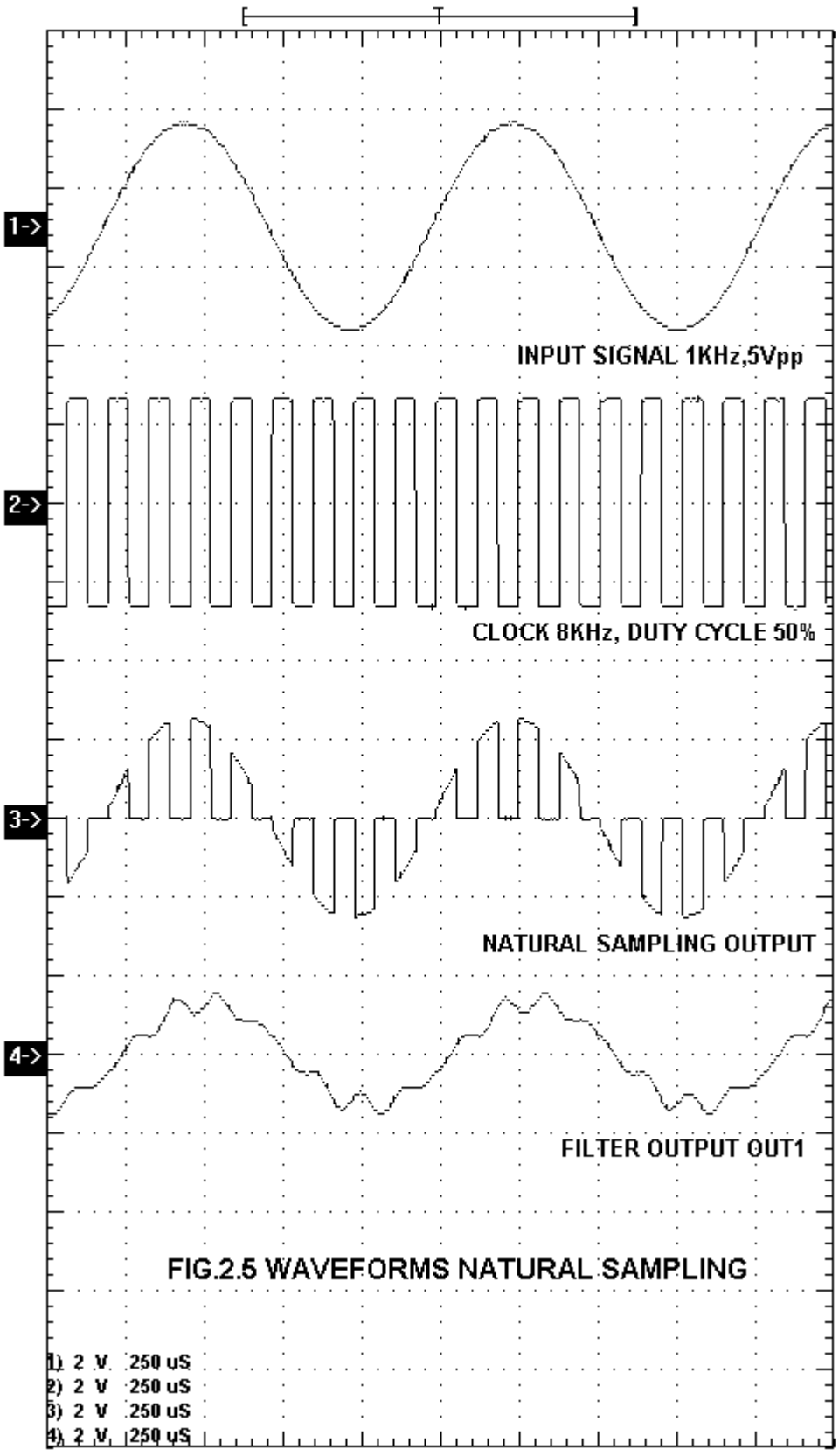


FIG.2.5 WAVEFORMS NATURAL SAMPLING

EXPERIMENT NO.3

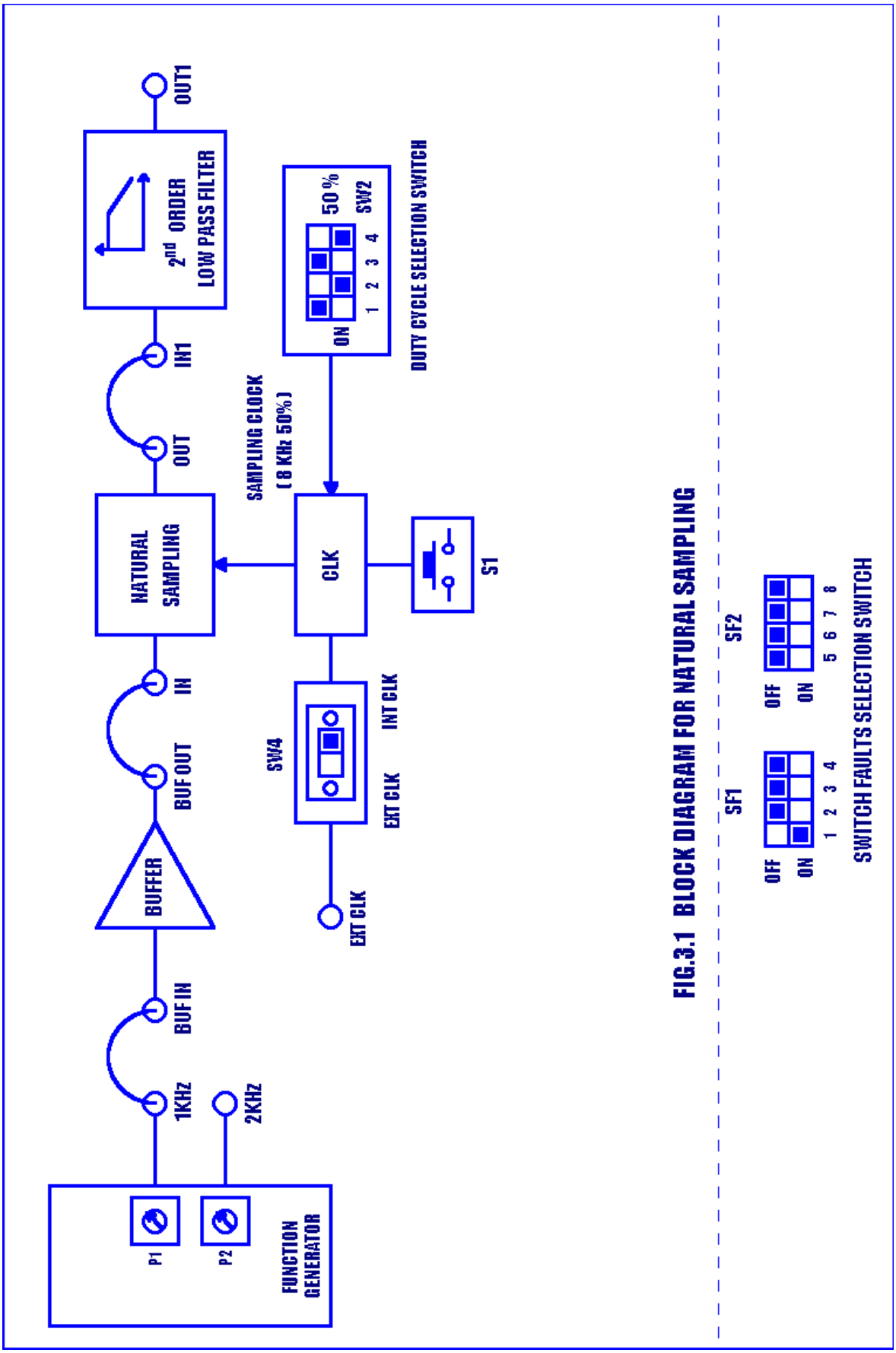


FIG.3.1 BLOCK DIAGRAM FOR NATURAL SAMPLING

EXPERIMENT NO: 3

NAME

Effect of Varying The Sampling Frequency Duty Cycle

OBJECTIVE

To study the effects of varying duty cycle of sampling frequency on the amplitude of the reconstructed signal

THEORY

Duty Cycle
The figure shows the functional block diagram of logic. The BCD counters counts from 0000 to 1001. This is connected to the A inputs of the comparator. The 4 way DIP switch can be configured such that the B inputs of the comparator varies from 0000 to 1001 and the frequency of the A<B output of the comparator is 10 times less than the frequency of the square wave, that is fed to the input of the BCD counter. Now the duty cycle of the A<B output of the comparator varies from 10% to 90% as the settings of the 4 way DIP switch varies from 0000 to 1001.

EQUIPMENTS

Experimenter kit DCL –01.
Connecting Chords
Power supply
20 MHz Dual Trace Oscilloscope

NOTE: Keep All The Switch Faults (Except Switch 1) In Off Position

PROCEDURE

1. Refer to the Block Diagram (Fig.3.1) & Carry out the following connections and switch settings.
2. Connect power supply in proper polarity to the kit **DCL-01** & switch it on.
3. Connect the **1 KHz**, 5Vpp Sine wave signal, generated on-board, to the **BUF IN** post of the BUFFER and **BUF OUT** post of the BUFFER to the **IN** post of the Natural Sampling block by means of the Connecting chords provided.
4. Connect the sampling frequency clock in the internal mode **INT CLK** using switch **SW4**.

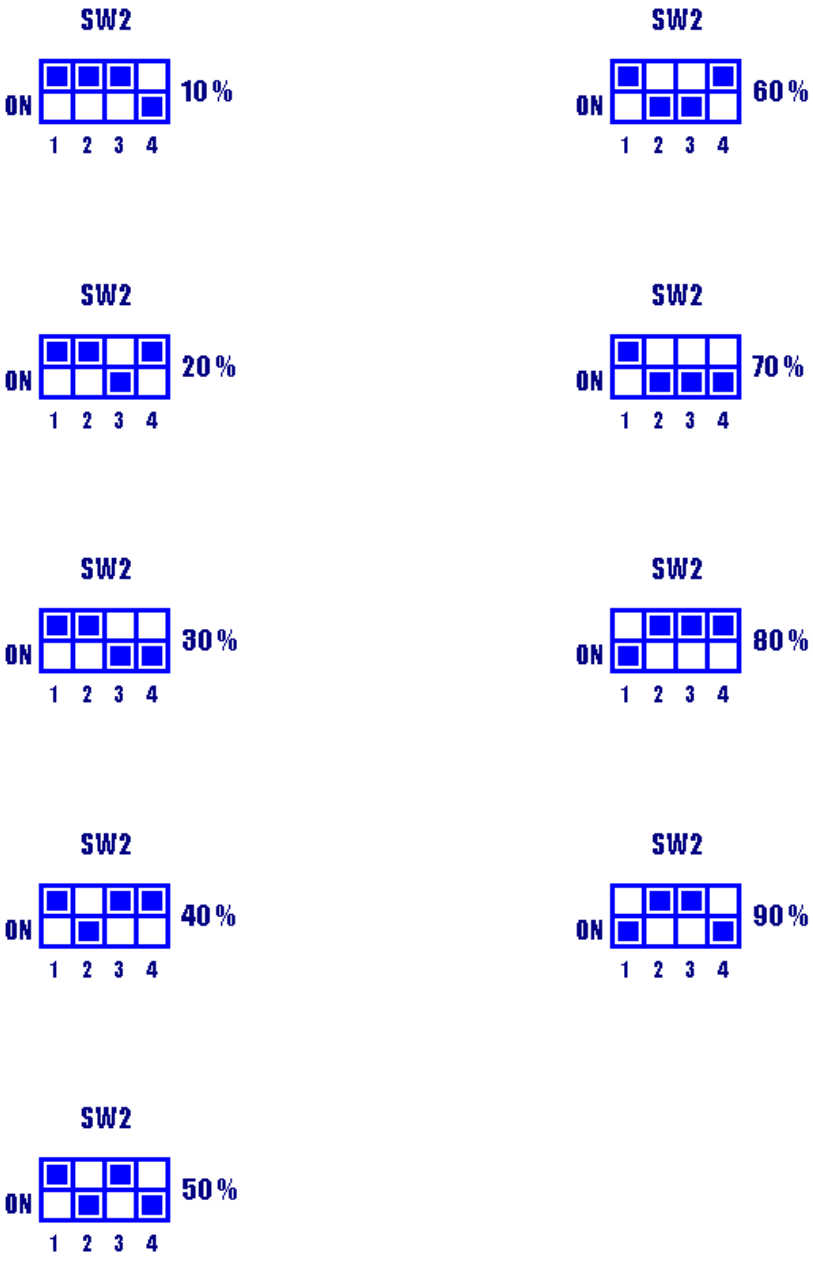


FIG.3.2 DUTY CYCLE SELECTION SWITCH

5. Using clock selector switch **S1** select **8 KHz** sampling frequency. Using switch **SW2** select duty cycle as shown in the switch setting diagram. (Fig. 3.2)
6. Connect sampled output **OUT** to the input **IN1** post of 2nd order Low Pass Butterworth Filter
7. Take observation as mentioned below for variation of duty cycle from 10 % to 90 % in steps of 10% as shown in switch setting diagram. (Fig. 3.2)
8. Similarly repeat the procedure for sample & hold circuit and flat top sample circuit.
9. Also observe waveforms by applying onboard 2KHz sine wave signal.

OBSERVATIONS

Observe the following waveforms in order for every setting and plot it on the paper.

- Analog Input waveform.
- Sampling frequency waveform with 90% duty cycle.
- Natural Sampled Signal and corresponding reconstructed output of 2nd order Low Pass Butterworth Filter. (Fig.3.3)
- Sampled and Hold signal output and corresponding reconstructed output of 2nd order Low Pass Butterworth Filter. (Fig.3.4)
- Flat top sample signal output and corresponding reconstructed output of 2nd order Low Pass Butterworth Filter. (Fig.3.5)
- Sampling frequency waveform with 10% duty cycle.
- Natural Sampled Signal and corresponding reconstructed output of 2nd order Low Pass Butterworth Filter. (Fig.3.6)
- Sampled and Hold signal output and corresponding reconstructed output of 2nd order Low Pass Butterworth Filter. (Fig.3.7)
- Flat top sample signal output and corresponding reconstructed output of 2nd order Low Pass Butterworth Filter. (Fig.3.8)

SWITCH FAULTS

Note: Keep the connections as per the procedure. Now switch corresponding fault switch button in ON condition & observe the different effect on the output. The faults are normally used one at a time.

- Put switch **6** of **SF2** in Switch Fault section to **ON** position. This will open B1 bit from the B input (4-bit DIP switch output) of the comparator. This introduces the fault in duty cycle section. With effect, change in duty cycle for settings (10%, 40%, 50%, 80% and 90%) will not be observed as expected.
- Put switch **7** of **SF2** in Switch Fault section to **ON** position. This will open the bypass capacitor of the 2nd order low pass butter-worth filter, which results in the induction of ripples at the filter output.
- Put switch **8** of **SF2** in Switch Fault section to **ON** position. This Removes the capacitor (C6) used in the generation of 1 KHz sine wave. Which makes the sine wave signal very distorted. The Observation can be made on this signal by changing the sampling frequencies and the duty cycle.

CONCLUSION

From the above observations, we conclude that as the duty cycle increases, the sampling time, i.e., the time period over which the signal information is obtained, is more. Hence the reconstructed Signal Amplitude approaches that of the original signal.

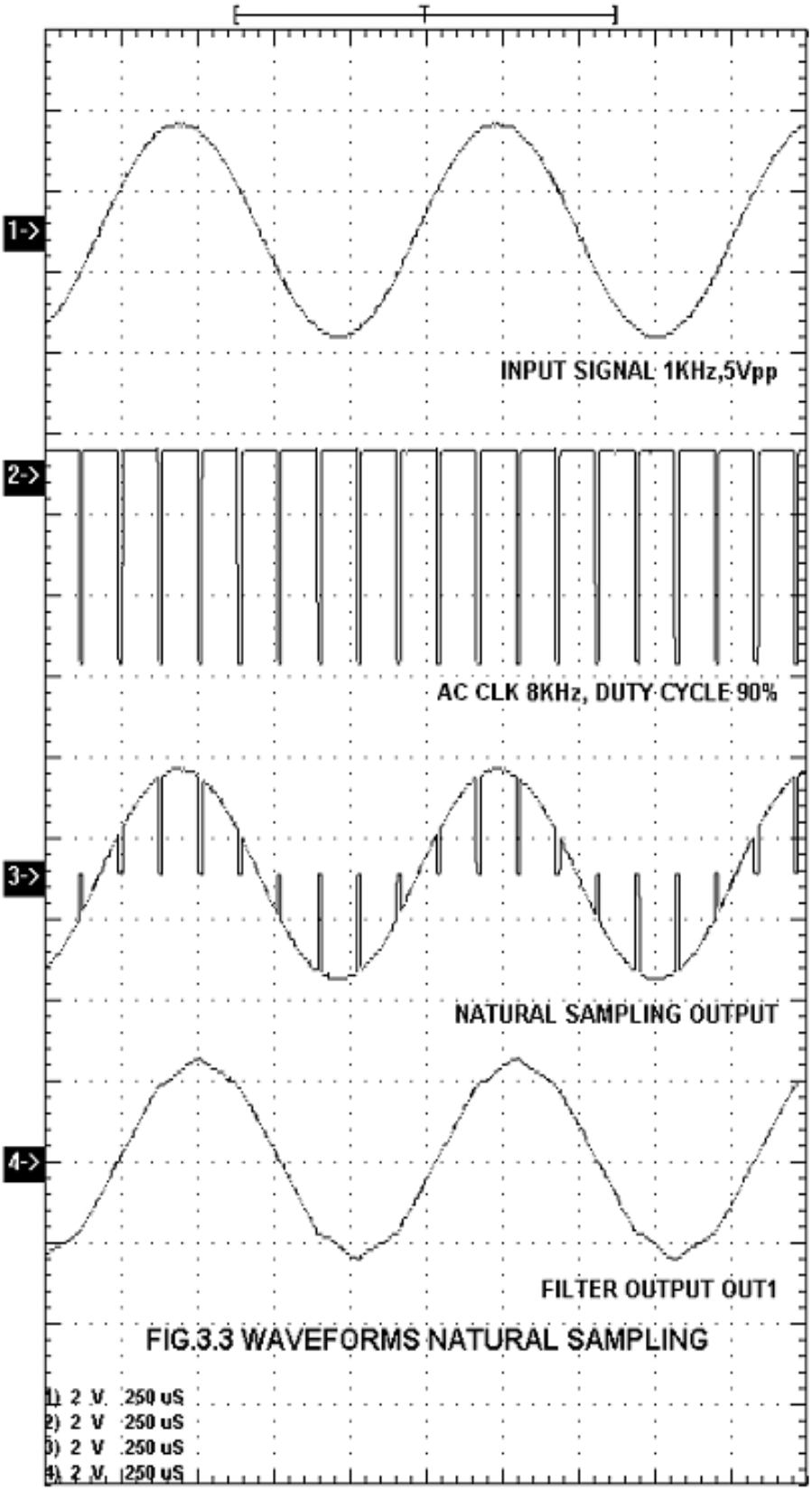


FIG.3.3 WAVEFORMS NATURAL SAMPLING

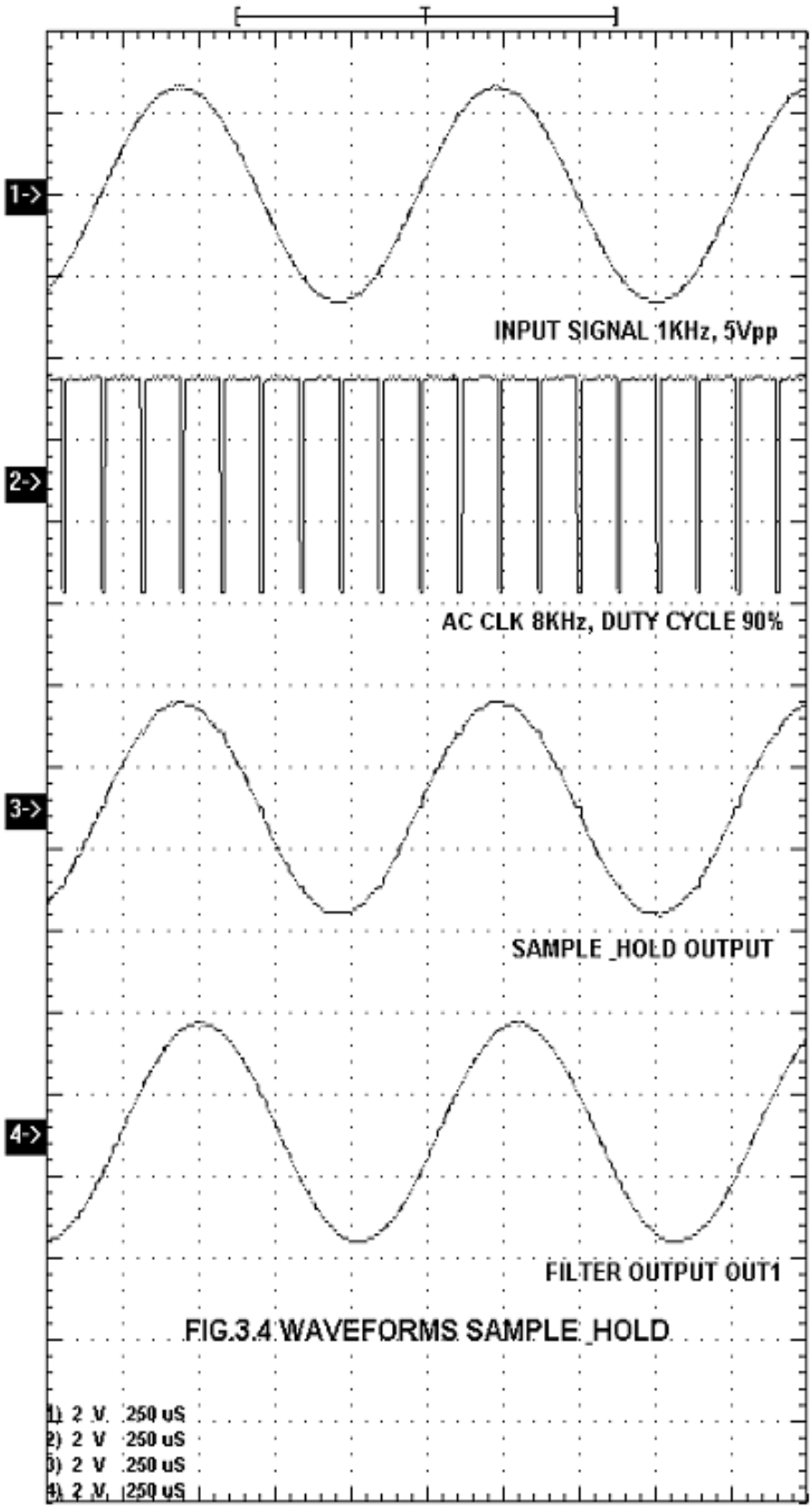


FIG.3.4 WAVEFORMS SAMPLE _HOLD

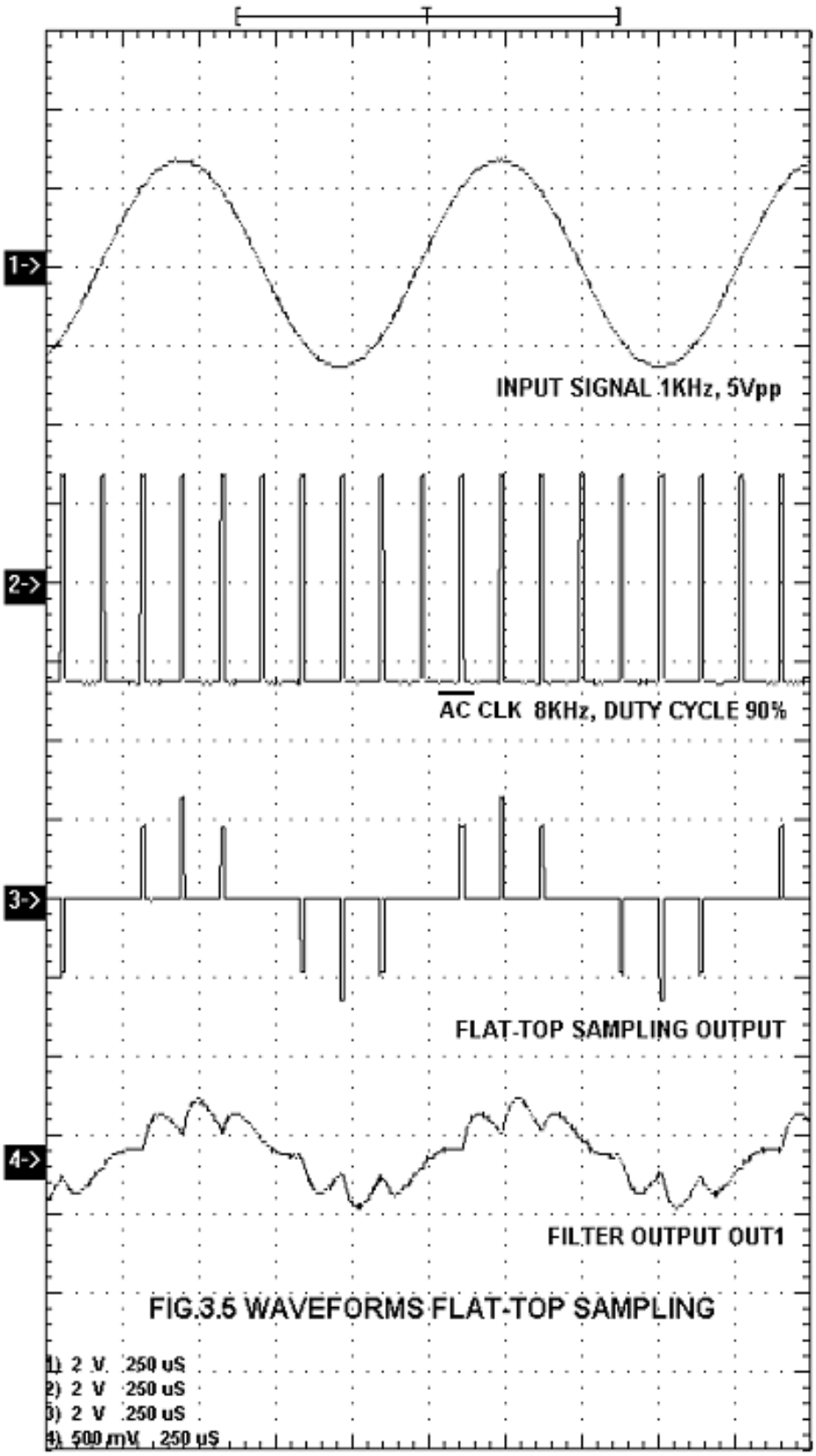


FIG.3.5 WAVEFORMS FLAT-TOP SAMPLING

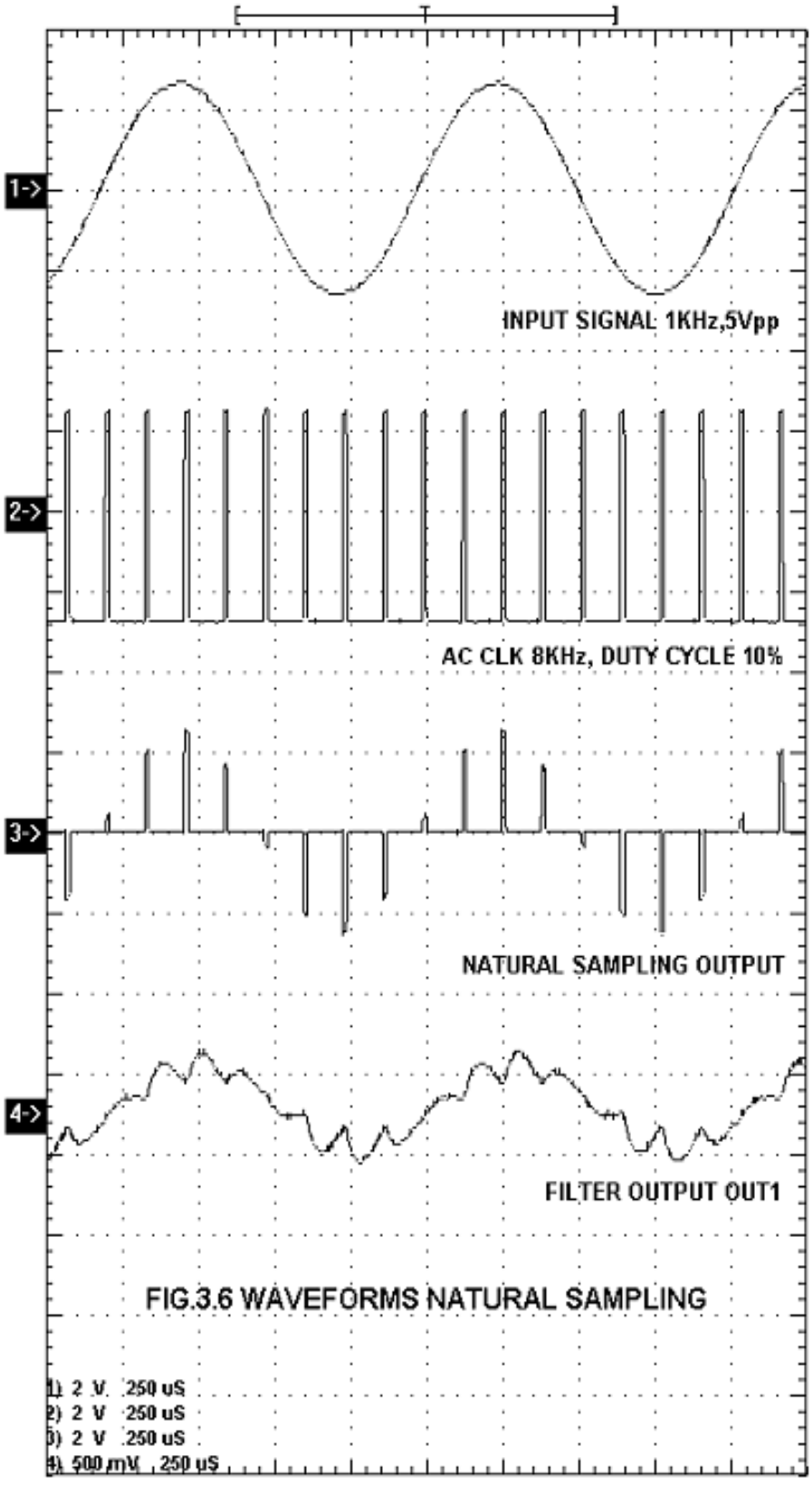


FIG.3.6 WAVEFORMS NATURAL SAMPLING

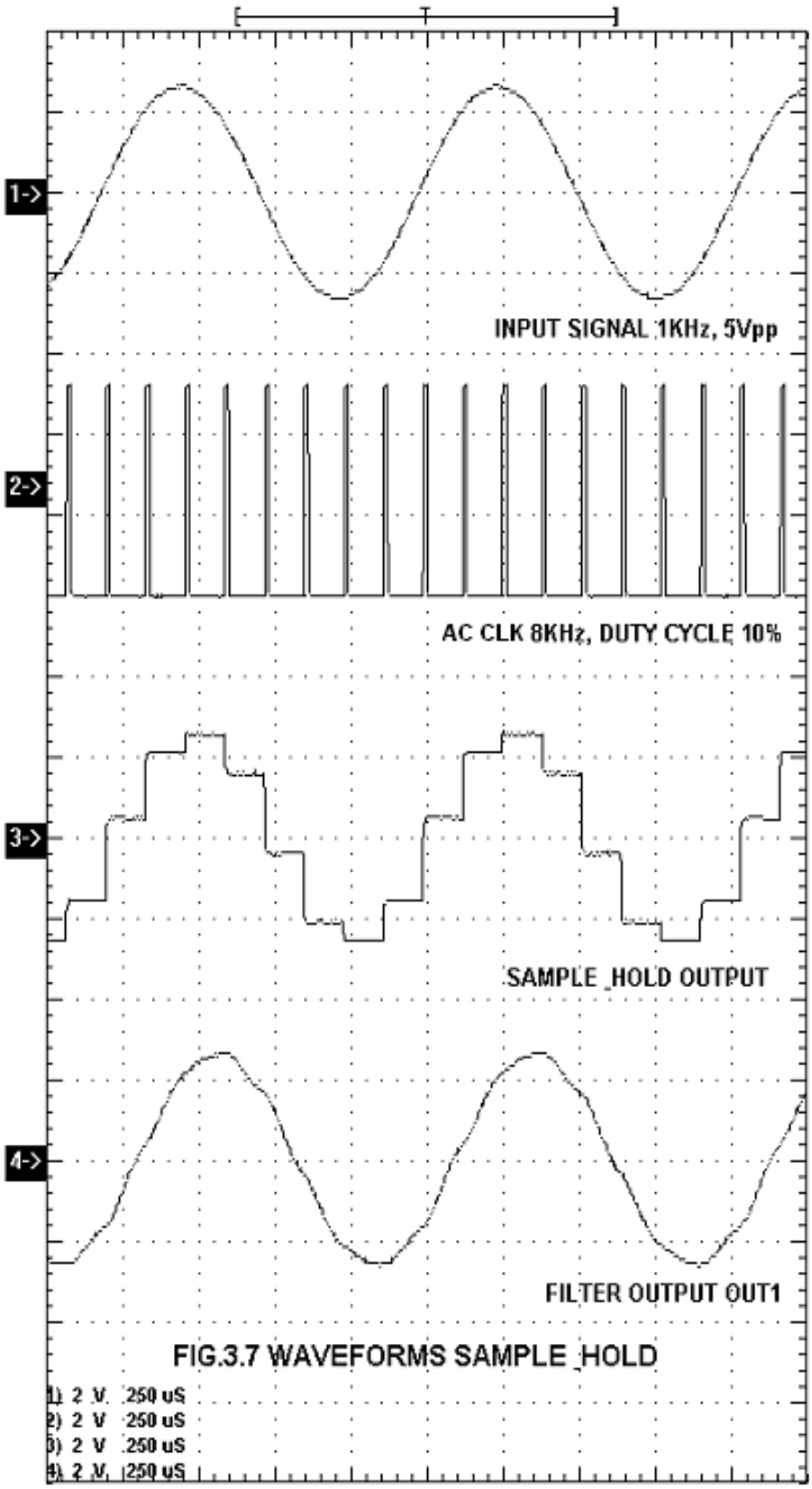


FIG.3.7 WAVEFORMS SAMPLE _HOLD

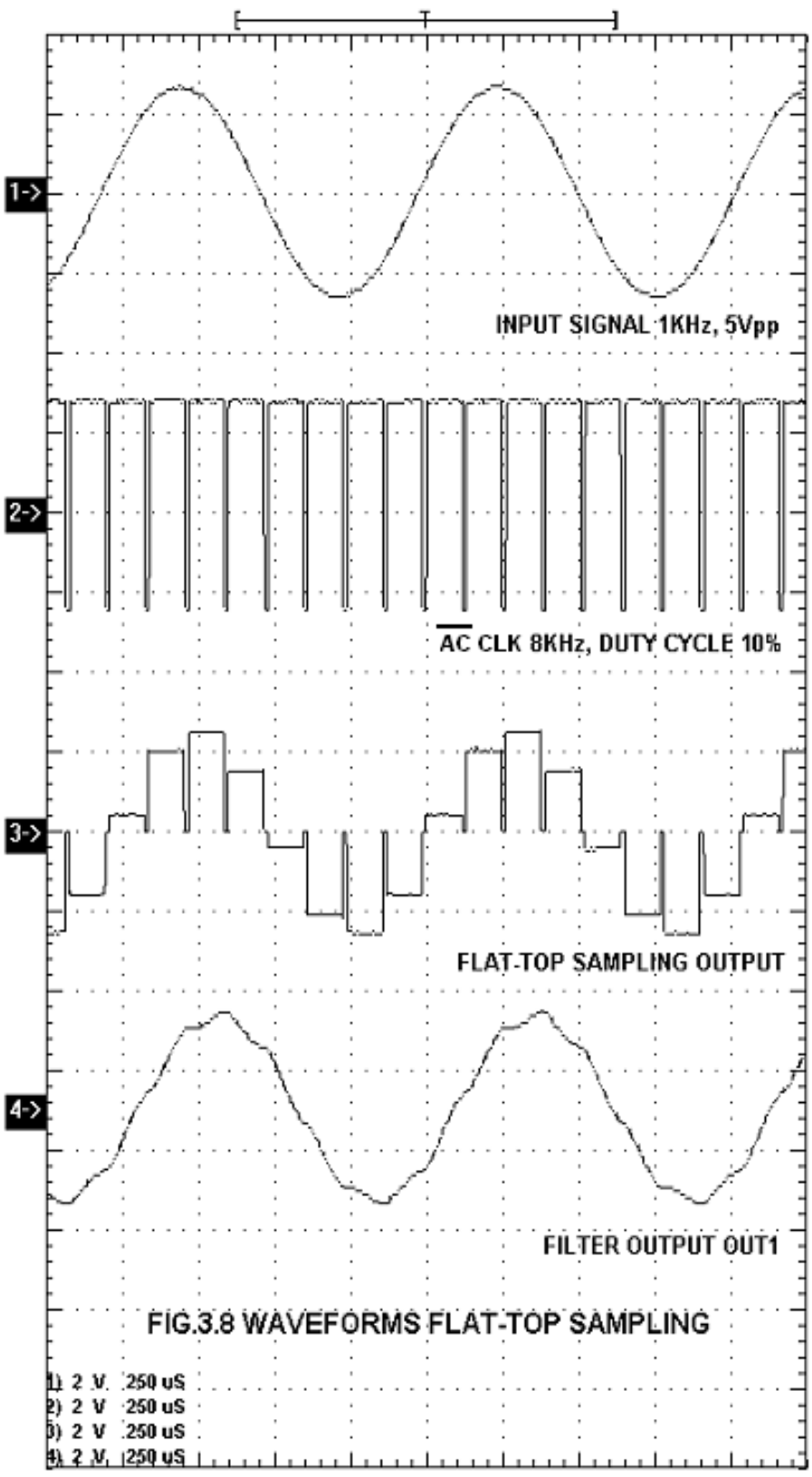


FIG.3.8 WAVEFORMS FLAT-TOP SAMPLING

EXPERIMENT NO.4

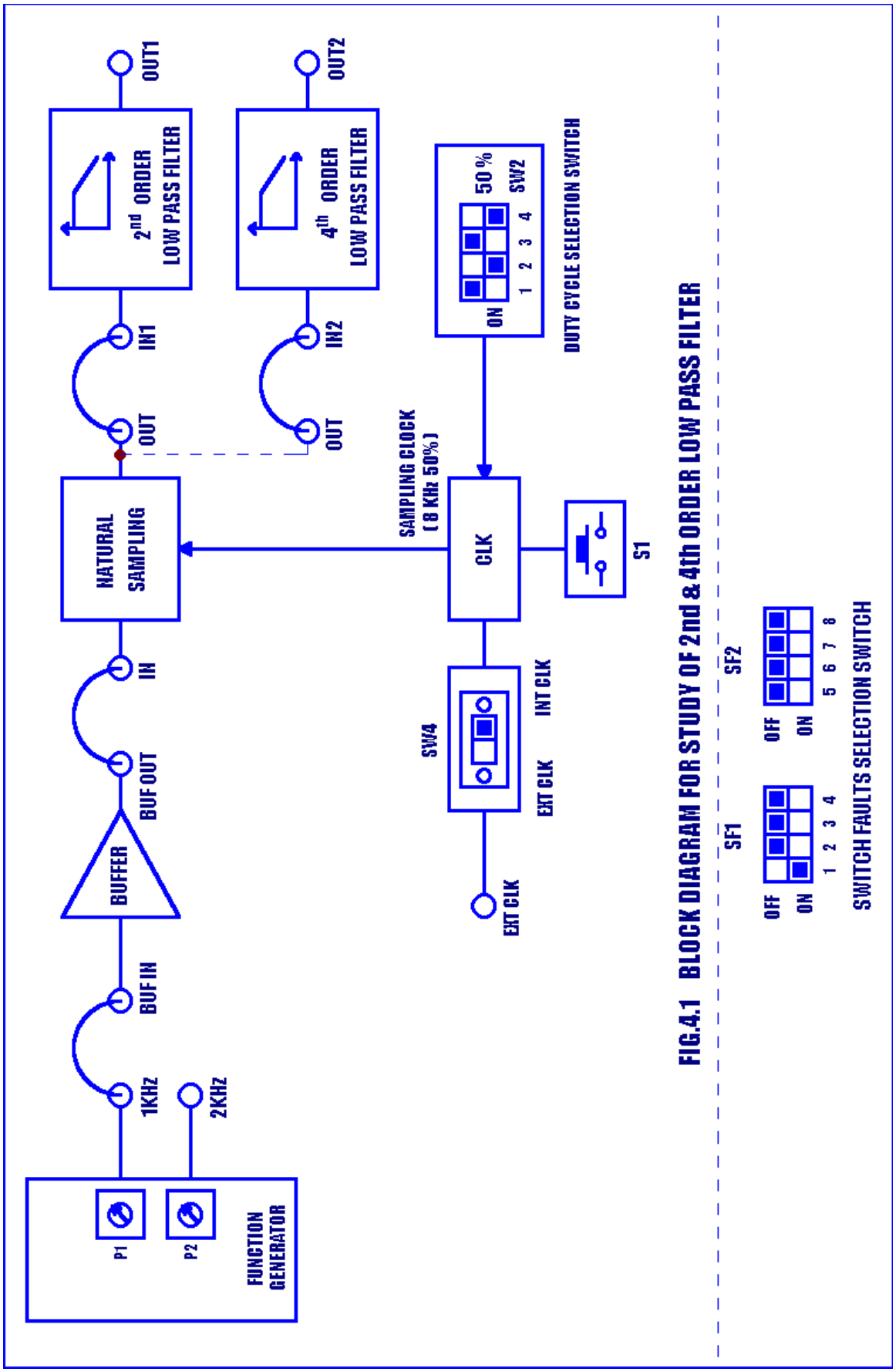


FIG.4.1 BLOCK DIAGRAM FOR STUDY OF 2nd & 4th ORDER LOW PASS FILTER

EXPERIMENT NO: 4

NAME

Study Of 2nd Order And 4th Order Low Pass Butterworth Filters

OBJECTIVE

To study the effect of 2nd Order and 4th Order Low Pass Butterworth Filters on the reconstruction of the signal.

THEORY

The reconstruction unit is basically a simple active Low Pass Butterworth Filter, which filters out the sampling frequency components from the samples and recovers the base band.

EQUIPMENTS

Experimenter kit DCL –01.
Connecting Chords
Power supply
20 MHz Dual Trace Oscilloscope

NOTE: Keep All The Switch Faults (Except Switch 1) In Off Position

PROCEDURE

1. Refer to the Block Diagram (Fig. 4.1) & Carry out the following connections and switch settings.
2. Connect power supply in proper polarity to the kit **DCL-01** & switch it on.
3. Connect the **1 KHz**, 5Vpp Sine wave signal, generated on board, to the **BUF IN** post of the BUFFER.
4. Connect the **BUF OUT** post to the **IN** post of the Natural Sampling block, by means of the Connecting chords provided.
5. Connect the sampling frequency signal in the internal mode **INT CLK** using switch **SW4**.
6. Using clock selector switches **S1**, select desired sampling frequency. The corresponding red LED indicates the selected sampling frequency.
7. Connect the Sampled Output post **OUT** to the input post **IN 1** of the 2nd Order Low Pass Butterworth Filter.
8. Using switch **SW2** select **50%** duty cycle.
9. Take necessary observation as mentioned below. Similarly Connect the Sampled Output post **OUT** to the input post **IN 2** of the 4th order Low Pass Butterworth Filter and take necessary observation.
10. Similarly repeat the procedure for sample & hold circuit and flat top sample circuit.
11. Also observe waveforms by applying onboard 2 KHz sine wave signal.

OBSERVATIONS

Observe the following waveforms in order for every setting and plot it on the paper.

- Analog Input waveform.
- Sampling frequency.
- Natural Sampled Signal and its corresponding reconstructed output of 2^{nd} order Low Pass Butterworth Filter. (Fig. 4.2)
- Natural Sampled Signal and its corresponding reconstructed output of 4^{th} order Low Pass Butterworth Filter. (Fig. 4.2)
- Sampled and Hold Signal and its corresponding reconstructed output of 2^{nd} order Low Pass Butterworth Filter. (Fig. 4.3)
- Sampled and Hold Signal and its corresponding reconstructed output of 4^{th} order Low Pass Butterworth Filter. (Fig. 4.3)
- Flat Top Sampled signal and its corresponding reconstructed output of 2^{nd} order Low Pass Butterworth Filter. (Fig. 4.4)
- Flat Top Sampled signal and its corresponding reconstructed output of 4^{th} order Low Pass Butterworth Filter. (Fig. 4.4)

SWITCH FAULTS

Note: Keep the connections as per the procedure. Now switch corresponding fault switch button in ON condition & observe the different effect on the output. The faults are normally used one at a time.

- Put switch **6** of **SF2** in Switch Fault section to **ON** position. This will open B1 bit from the B input (4-bit DIP switch output) of the comparator. This introduces the fault in duty cycle section. With effect, change in duty cycle for settings (10%, 40%, 50%, 80% and 90%) will not be observed as expected.
- Put switch **7** of **SF2** in Switch Fault section to **ON** position. This will open the bypass capacitor of the 2^{nd} order low pass butter-worth filter, which results in the induction of ripples at the filter output.
- Put switch **8** of **SF2** in Switch Fault section to **ON** position. This Removes the capacitor (C6) used in the generation of 1KHz sine wave. Which makes the sine wave signal very distorted. The Observation can be made on this signal by changing the sampling frequencies and the duty cycle.

CONCLUSION

When the output waveform of the above two cases are observed on the scope, we observe that as the Order of the filter increases, the reconstructed signal characteristics also improve.

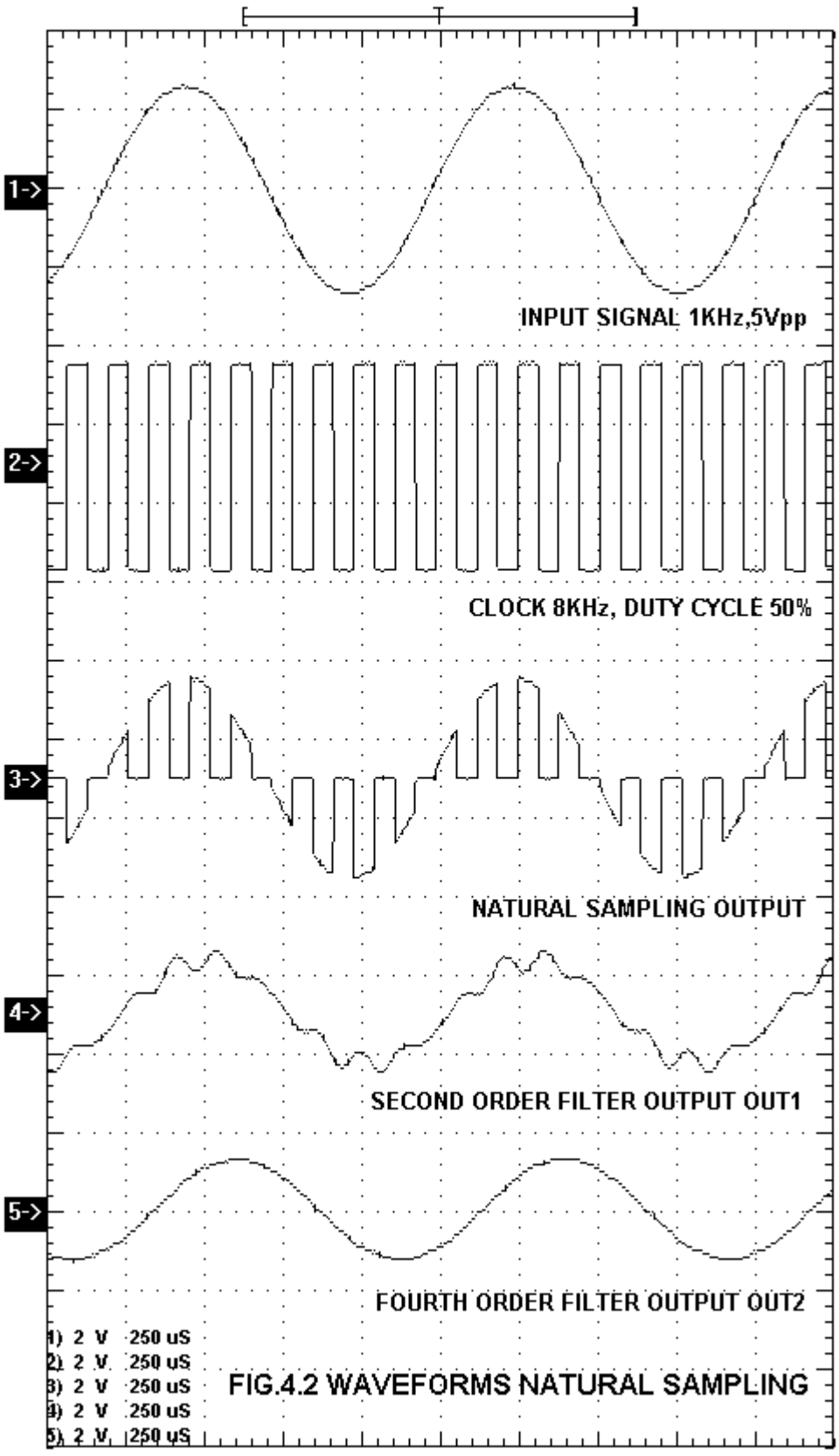


FIG.4.2 WAVEFORMS NATURAL SAMPLING

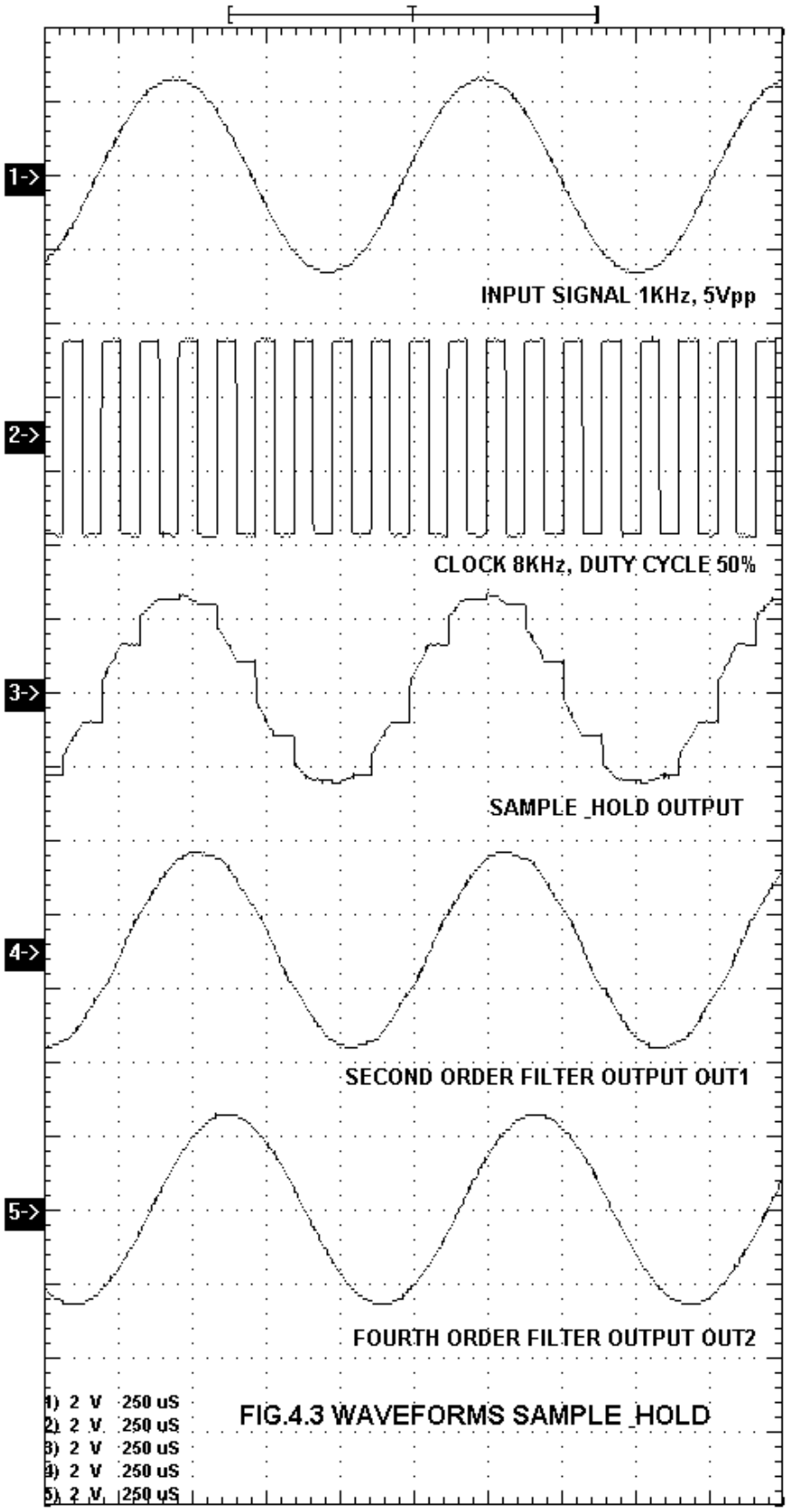


FIG.4.3 WAVEFORMS SAMPLE _HOLD

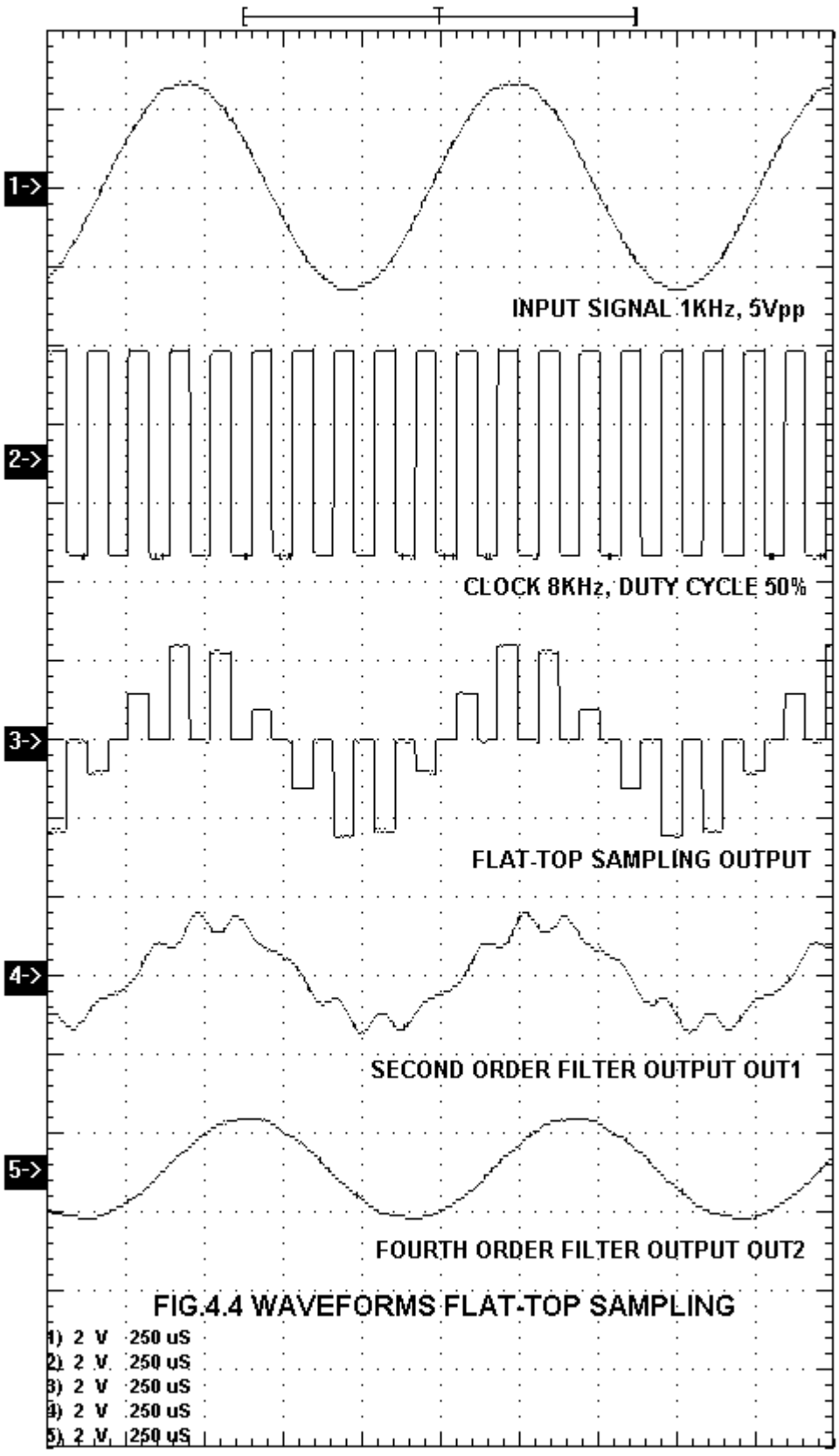


FIG.4.4 WAVEFORMS FLAT-TOP SAMPLING

EXPERIMENT NO.5

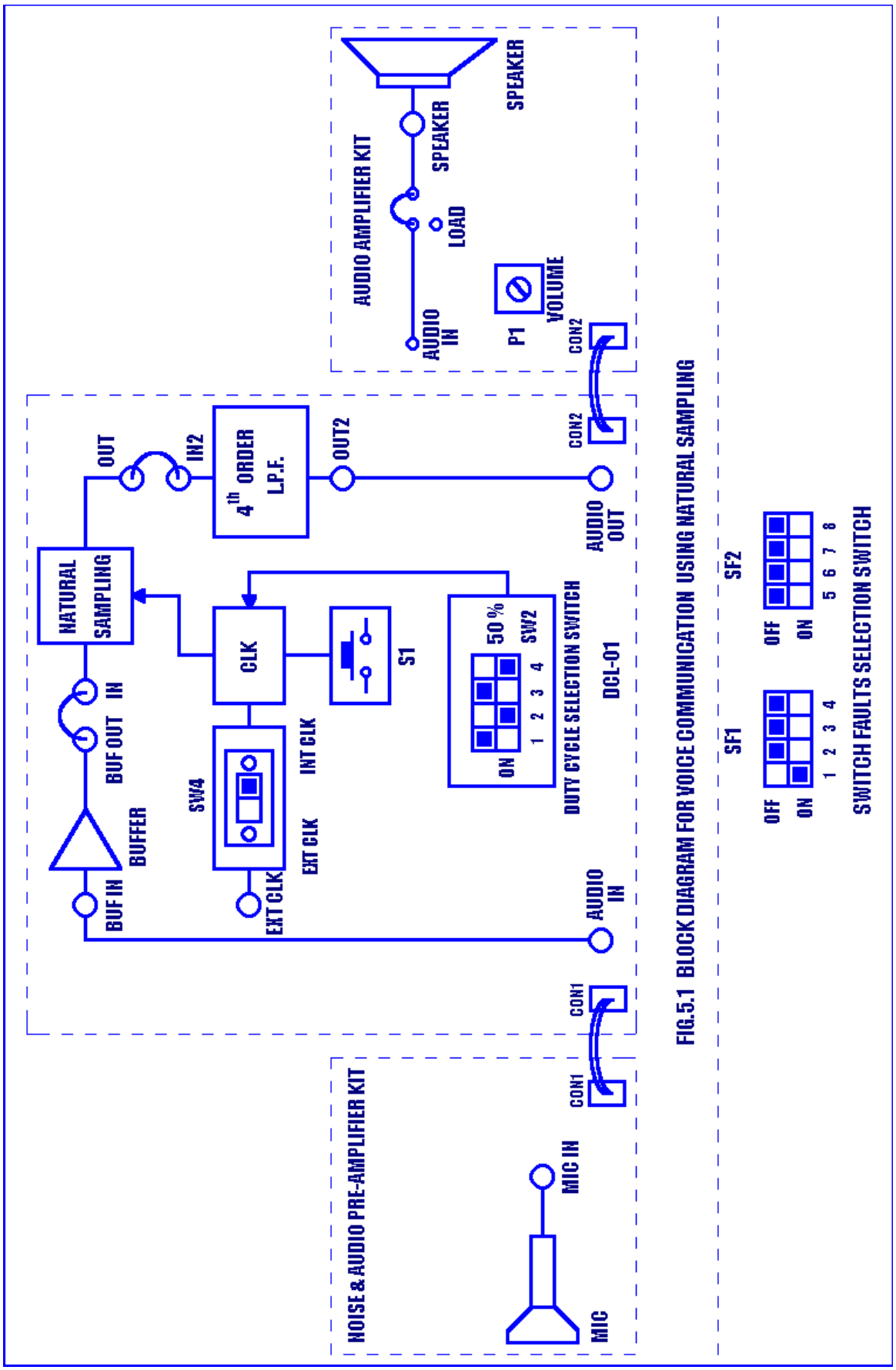


FIG.5.1 BLOCK DIAGRAM FOR VOICE COMMUNICATION USING NATURAL SAMPLING

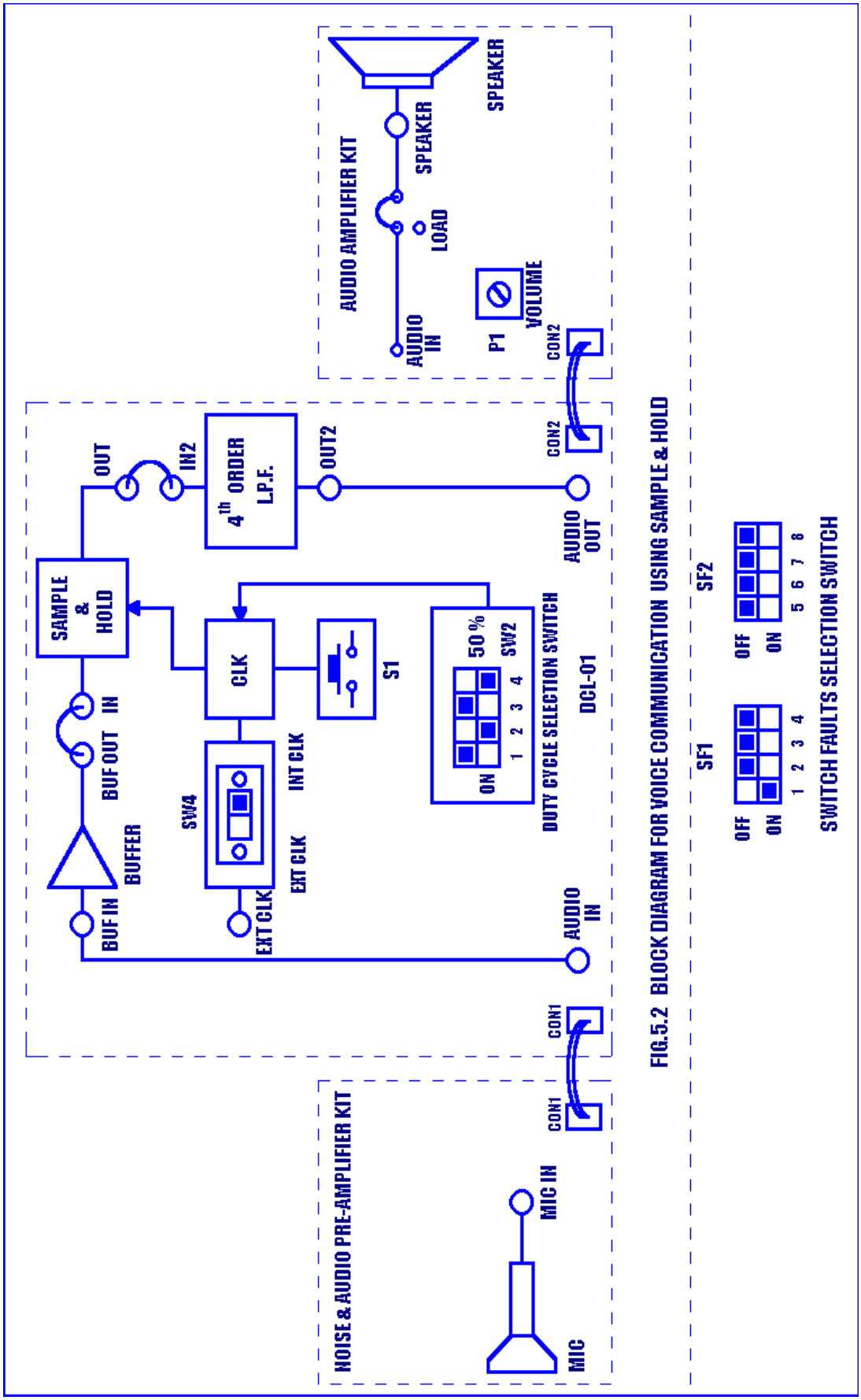


FIG.5.2 BLOCK DIAGRAM FOR VOICE COMMUNICATION USING SAMPLE & HOLD

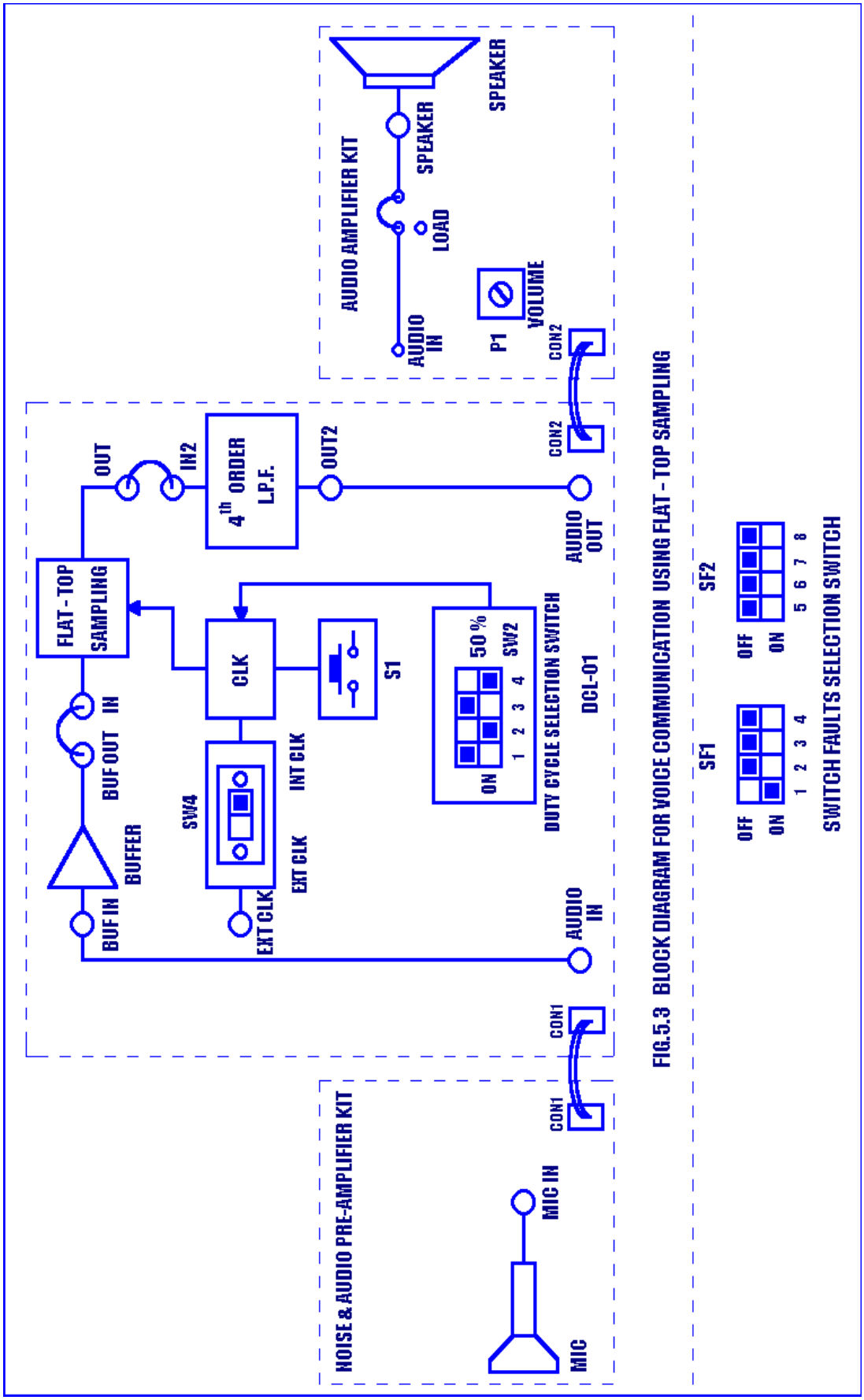


FIG.5.3 BLOCK DIAGRAM FOR VOICE COMMUNICATION USING FLAT - TOP SAMPLING

EXPERIMENT NO: 5

NAME

Voice Communication Using All The Three Sampling Techniques

OBJECTIVE

Study of Voice communication using Natural sampling, Sample and Hold, and Flat Top Sampling Techniques

THEORY

Voice being analog signal is sampled by using any one method at transmitter end and reconstructed using filter of different order like the 2^{nd} and 4^{th} order low pass butter-worth filter at receiver side. For performing the Voice communication, set up the basic Natural, Sample and Hold and Flat Top Sampling Experiment as mentioned earlier and then feed voice signal as input and the reconstructed output to speaker.

EQUIPMENTS

Experimenter kit DCL –01.
Connecting Chords
Power supply
20 MHz Dual Trace Oscilloscope
Microphone
Noise and Audio Pre-Amplifier kit
Audio Amplifier kit
Power connection cables

NOTE: Keep All The Switch Faults (Except Switch 1) In Off Position

PROCEDURE

1. Refer to the Block Diagram (Fig. 5.1) & Carry out the following connections and switch settings.
2. Connect the Noise and Audio Pre-Amplifier kit to the **CON1** Post on **DCL-01** kit using power connection cable.
3. Connect the Audio Amplifier kit to the **CON2** Post on **DCL-01** kit using power connection cable.
4. Connect power supply in proper polarity to the kit **DCL-01** & switch it on.
5. Connect Microphone to the post **MIC IN** on Noise and Audio Pre-Amplifier kit.
6. Connect the input signal from **AUDIO IN** Post to **BUF IN** Post of the BUFFER.
7. Connect the **BUF OUT** post of the BUFFER to the **IN** post of the Natural Sampling block.

8. Connect the sampling frequency clock in the internal mode **INT CLK** using switch **SW4**.
9. Using clock selector switch **S1** select **8 KHz** sampling frequency.
10. Using switch **SW2** select **50%** duty cycle.
11. Connect the **OUT** post of the Natural sampling block to the input **IN2** post of the 4^{th} Order Low Pass Butterworth Filter.
12. Connect the output signal from **OUT 2** of the 4^{th} order low pass butter-worth filter to post **AUDIO OUT**.
13. Put the jumper in Audio Amplifier Kit towards speaker selection as shown in Fig. 5.1.
14. Connect the speaker provided with the kit to the speaker jack on Audio Amplifier Kit.
15. Repeat voice link through Sample and Hold (Fig. 5.2) & Flat Top sampling (Fig. 5.3) techniques by referring the experimental procedure of the same.

CONCLUSION

When the outputs are observed, we observe that for Sample and Hold voice communication audio response is better than Natural sample & Flat top Sample voice communication.